A 10-Gbps Continuous-Time Linear Equalizer for mm-Wave Dielectric Waveguide Communication

Oscar E. Mattia, *Member, IEEE*, Mahmoud Sawaby, *Graduate Student Member, IEEE*, Kevin Zheng, *Member, IEEE*, Amin Arbabian, *Senior Member, IEEE*, and Boris Murmann, *Fellow, IEEE*

***Abstract*—The data rate-times-distance product in mm-wave dielectric waveguide (DWG) communication links is usually limited by waveguide dispersion. This letter presents the DWG's baseband impulse response in the context of a homodyne receiver and introduces a continuous-time linear equalizer able to minimize such dispersion. The desired transfer function is implemented with inverter-based transconductance cells. The simulation and measurement results at 10-Gbps data rate show eye-opening improvement at two distances (10 and 15 m) and carrier frequencies (140 and 160 GHz). The equalizer occupies 80 × 32 μm^2 in GLOBALFOUNDRIES 22-nm FD-SOI.**

***Index Terms*—Continuous-time linear equalizer (CTLE), dielectric waveguide (DWG), equalization, mm-wave communication, wireless-over-fiber.**

I. Introduction

The demand for communication capacity continues to increase exponentially, driven by mobile and Web applications, such as 5G wireless communication and machine learning workloads. Electrical links today achieve more than 100 Gbps [1], but their reach is limited to on-chip and onboard distances due to copper attenuation, dispersion, and impedance discontinuities. Advanced digital signal processing has been used to address the more demanding equalization and forward-error-correction requirements of longer channels, penalizing the transceiver area and power consumption. Optical links, on the other hand, provide a higher quality channel that allows long-reach off-board communication. However, the precision packaging, electrical-to-optical, and optical-to-electrical conversion incur a significant cost and density overhead. Off-board communication is also possible with mm-wave wireless, that has large available bandwidth and is now feasible in CMOS technologies. However, the high free-space path loss requires the use of phased arrays to form directional beams, which limits the power efficiency and density of the link.

An alternative to these traditional media is a dielectric waveguide (DWG) made of plastic. It has been proposed as a cheap and simple interconnect for short to medium range links (1–20 m) [2], [3]. In addition, the transducer from silicon IC to DWG can be entirely integrated using simple electromagnetic means and standard CMOS processing. The fundamental physical constraints and link tradeoffs, such as carrier frequency and DWG length have been covered in [4], where a theoretical capacity study has shown that the data rate-times-distance product is usually limited by waveguide dispersion instead of attenuation, and a recent survey of DWG transceivers reflects this limitation [5]. We note that equalization for DWG links has not received much attention, so in this letter, we propose a programmable continuous-time linear equalizer (CTLE) for DWG dispersion. The CTLE is an important building block to enable higher data rate-times-distance product in the context of a homodyne QPSK transceiver, as shown in Fig. 1. A parametric DWG pulse response model allows us to explore different distance and carrier frequencies, and is presented in Section II. The inverter-based CTLE is proposed in Section III. The measurement results are shown in Section IV.

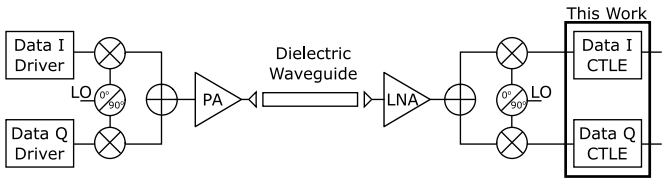

Fig. 1. Homodyne transceiver and proposed equalizer location.

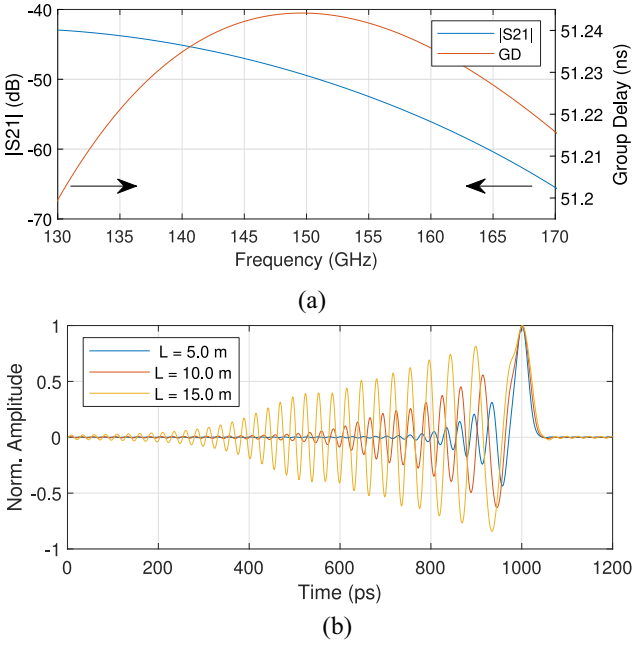

Fig. 2. DWG model. (a) Frequency response for $L = 10$ m. (b) Real baseband impulse response for varying length L.

II. Dielectric Waveguide Model

Dispersion in single-mode DWG originates from material dispersion and waveguide dispersion. Material dispersion, due to frequency-dependent variations of the material relative permittivity and magnetic permeability (ε_r and μ_r), is negligible for common low-loss dielectric materials (such as Teflon, HDPE, and LDPE). Waveguide dispersion, on the other hand, is strongly frequency dependent and affected by DWG dimensions and geometry, as

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Oscar E. Mattia, Mahmoud Sawaby, Amin Arbabian, and Boris Murmann are with the Electrical Engineering Department, Stanford University, Stanford, CA 94035 USA (e-mail: omattia@stanford.edu).

Kevin Zheng is with the Wired and Wireless Group, Xilinx Inc., San Jose, CA 95124 USA.

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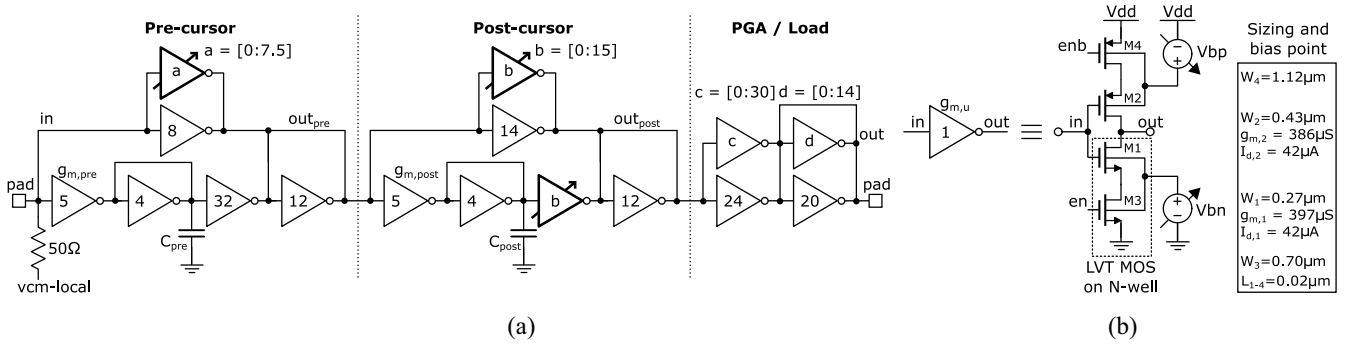

Fig. 3. DWG CTLE. (a) Single-ended block diagram. (b) $g_{m,u}$ unit cell schematic.

well as the absolute magnitude of the material properties [4]. To investigate the impulse response of the DWG, a 1-m rectangular rod with 1×1 mm^2 cross section and $\varepsilon_r = 2.1$ was used. The attenuation constant α was obtained from [3], and the propagation constant β was estimated through numerical methods [6]. Equation $S_{21}(f) = \exp[-(\alpha(f) + j\beta(f))\cdot L]$ provides a parametric model where the DWG length L was varied from 5 to 15 m. The frequency response for $L = 10$ m is shown in Fig. 2(a).

With increasing frequency, the electric field energy confinement in the DWG increases. The increased confinement results in higher absolute group delay (GD) due to higher effective permittivity, but with less GD variation due to the more homogeneous medium [4]. As the frequency increases further, the energy is confined in a smaller part of the cross section of the DWG, which leads to a drop in the GD. In the context of a homodyne quadrature receiver, after down-conversion to baseband, these faster components would appear in the form of ringing before the main cursor. The resulting real part of the baseband impulse response (normalized to the peak cursor value at 1.000 ps) is presented in Fig. 2(b) for a 140-GHz carrier frequency example and varying length L. The CTLE proposed in the next section was designed to cover a range of carrier frequencies and waveguide dimensions, with programmable precursor and postcursor equalization.

III. Continuous Time Linear Equalizer

Inverter-based g_m cells are gaining traction in commercial wireline receivers due to their area and bandwidth advantages [1]. In [7], a 5-tap $T_S/2$ analog-FFE has been implemented, where the delay cell is a first-order pole-zero Pade approximant. In [8], additive and subtractive CTLE topologies for high-frequency boosting were compared. In this letter, a combination of these techniques is used to equalize both precursor and postcursor pulse response, through a two-stage subtractive topology. A third stage implements programmable gain amplifier (PGA) and 50-Ω output load matching, for testing purposes. The single-ended block diagram is shown in Fig. 3(a). The transconductance unit cell $g_{m,u}$ is shown in Fig. 3(b), and the circuit implementation is pseudodifferential.

The precursor stage transfer function is approximated by (1), where $\tau_{\text{pre}} = g_{m,\text{pre}}/C_{\text{pre}}$, being $g_{m,\text{pre}} = 5g_{m,u}$ and assuming zero output conductance. The inverting path with coefficient a subtracts from the low-pass noninverting path, resulting in a programmable right-half plane (RHP) zero. The amount of equalization is given by the driving strength difference between both paths, and is programmed by coefficient a, that has resolution of 0.5 $g_{m,u}$ and maximum value of 7.5 $g_{m,u}$. This transfer function can be seen as a precursor low pass that damps the precursor ringing of Fig. 2(b)

$$H_{\text{pre}}(s) = \left[\frac{(\frac{32-a}{12}) - (\frac{8+a}{12})s\tau_{\text{pre}}}{1 + s\tau_{\text{pre}}}\right] P_{\text{pre}}(s). \tag{1}$$

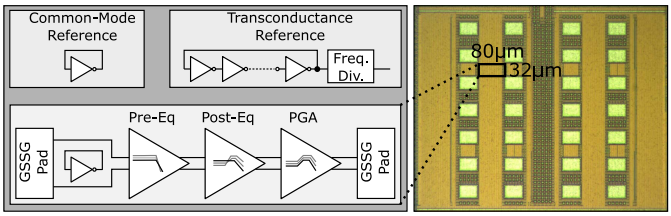

Fig. 4. DWG equalizer chip block diagram and die micrograph.

The postcursor stage transfer function is approximated by (2), where the dominant pole time constant $\tau_{\text{post}} = g_{m,\text{post}}/C_{\text{post}}$, being $g_{m,\text{post}} = 5g_{m,u}$. It consists of a programmable left-half plane (LHP) zero through coefficient b, that is present on both inverting and noninverting paths. Coefficient b has resolution of 1 $g_{m,u}$ and maximum value of 15 $g_{m,u}$. There is also small influence of b on the dc gain

$$H_{\text{post}}(s) = \left[\frac{(\frac{14}{12} - \frac{5b}{48}) + (\frac{14+b}{12})s\tau_{\text{post}}}{1 + s\tau_{\text{post}}}\right] P_{\text{post}}(s). \tag{2}$$

In both (1) and (2), the $P(s)$ terms represent a higher frequency parasitic pole due to subsequent stage loading and wiring parasitics. These parasitic time constants are designed to be much faster than the dominant pole's time constant. Programmable gain is implemented on the third stage through factor c, that can assume a maximum value of 30 $g_{m,u}$. Programmable 50-Ω load matching is implemented through factor d, which can assume a maximum value of 14 $g_{m,u}$. Thermometer coding on the MSB of coefficients a, b, and c ensures monotonicity in the presence of a random mismatch.

The transconductance unit cell $g_{m,u}$ size and nominal operating point are shown in Fig. 3(b). Transistors $M1$ and $M2$ are an inverter-based transconductor, while transistors $M3$ and $M4$ act as switches, enabling or disabling the unitary cell. The use of an nMOS low-VT transistor on an N-well allows forward body biasing (FBB) with positive supply only, simplifying the power domains design. The pMOS transistors are standard-VT on N-well devices. This device threshold choice results in a larger imbalance between the pMOS and nMOS drive strengths, which impacts bandwidth, but is considered a worthy tradeoff for the target of 10 Gbps. Off-chip voltage sources V_{bp} and V_{bn} are used to compensate for process, voltage, and temperature (PVT) variations, with nominal value of $V_{dd}/2$ and range of $[0 \cdots V_{dd}]$. The back-gate control of threshold voltage in the independent multigate 22-nm FD-SOI technology offers fundamental dynamic range advantages over single-gate or connected multigate (e.g., FinFET) inverter-based transconductors, because control is independent of supply voltage and not in the signal path.

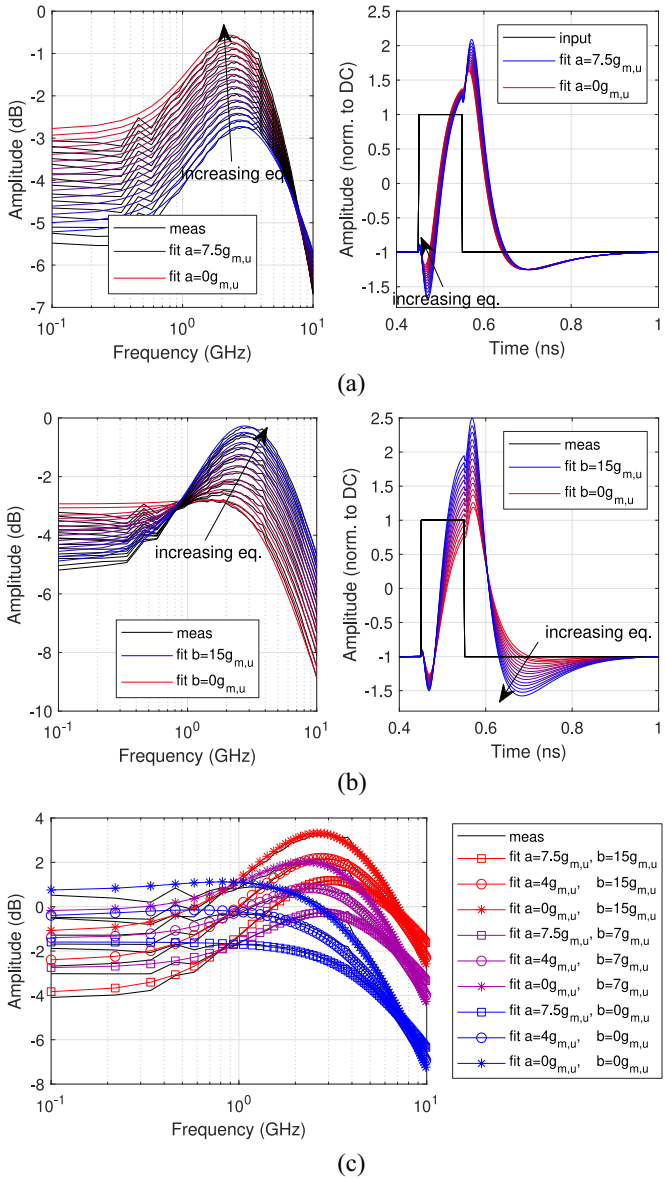

Fig. 5. Measured equalizer frequency response and fitted pulse response: (a) precursor; (b) postcursor; and (c) combined.

IV. Measurement Results

The equalizer was fabricated in GLOBALFOUNDRIES 22-nm FD-SOI technology. A block diagram of the chip and the respective die micrograph is shown in Fig. 4. The equalizer active area is only $80 \times 32\ \mu\text{m}^2$, and GSSG pads are used to probe the high-speed input and output analog signals. The inputs are ac coupled and the common mode is set by a diode-connected inverter. PVT monitoring structures provide common-mode voltage and absolute g_m references.

The equalizer S_{21} frequency response was measured on-die with an R&S ZVA67 vector network analyzer, where cables and probes have been de-embedded with the use of a calibration substrate. Fig. 5(a) shows the precursor tuning range with minimum postcursor equalization. Fig. 5(b) shows the postcursor tuning range with minimum precursor equalization. The combined equalization capability is shown in Fig. 5(c). The precursor has a tuning range of 3 dB (precursor equalization is strongest at min-code, or $a = 0$), and the postcursor has a tuning range of 4 dB with the nominal peaking frequency of 3 GHz. The measured PGA tuning range is 6 dB,

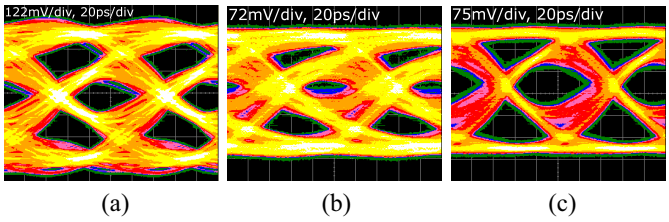

Fig. 6. Measured 10-Gbps baseband eye diagrams for $f_c = 160$ GHz and $L = 10$ m: (a) through; (b) equalizer output at $a = 7.5$ and $b = 0$; and (c) equalizer output at $a = 4$ and $b = 8$.

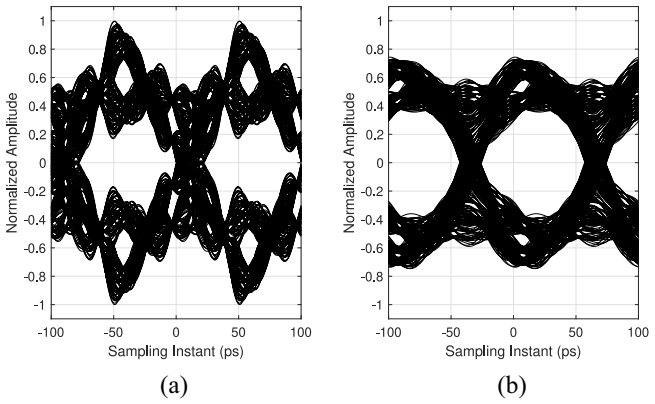

Fig. 7. Simulated 10-Gbps baseband eye diagrams for $f_c = 140$ GHz and $L = 15$ m: (a) normalized DWG output and (b) equalizer output for codes $a = 4$ and $b = 8$, based on fitted measurement results.

and the worst-case output matching is -12 dB up to 10 GHz (not shown). The measured frequency response was fitted to a fourth-order rational function, from which the pulse response was extracted and normalized to the dc value, to emphasize the effect of equalization.

A. Link Emulation

A Keysight M8195A arbitrary waveform generator (AWG) emulates the baseband PRBS-9 sequence convolved with a 10-m DWG real baseband impulse response at 160-GHz carrier frequency. The eye diagrams are measured with Agilent's N9403B BER tester, and shown in Fig. 6. A thorough measurement was performed to verify the eye quality, shown in Fig. 6(a), since there are limitations with the time-domain generation of the high-frequency precursor ringing. Namely, the model impulse response was resampled from 200 to 64 GS/s to comply with the AWG sampling frequency, and the finite rise/fall time of 18 ps. The input signal amplitude is 440 $\text{mV}_{pp,\text{diff}}$ (-3 dB back-off from the CTLE's input-referred 1-dB compression point). The output eye at minimum equalization ($a = 7.5$, $b = 0$) is shown in Fig. 6(b). Coefficients a and b were then swept, and the residual ISI (estimated by the $+1/-1$ level variation) was minimized for codes $a = 4$, $b = 8$, shown in Fig. 6(c).

The effectiveness of precursor equalization can also be demonstrated numerically by using the equalizer's fitted transfer function of Fig. 5 and the parametric DWG model of Fig. 2(b). The eye-opening improvement at baseband was estimated using different carrier frequencies and DWG lengths. Shown in Fig. 7 are simulation results for a PRBS-9 input sequence at 140-GHz carrier frequency, 15-m length, and 10-Gbps data rate. The DWG baseband output, shown in Fig. 7(a), is noiseless and was normalized to verify the effect of dispersion only. Fig. 7(b) shows 2X vertical eye-opening improvement at the equalizer output, for codes $a = 4$ and $b = 8$.

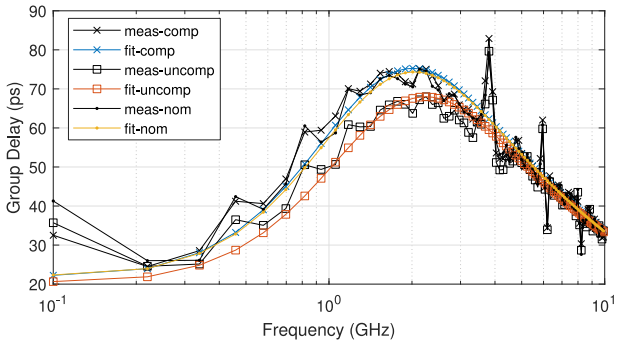

Fig. 8. Body bias compensation of GD frequency response.

TABLE I
RECENTLY PUBLISHED INVERTER-BASED CTLES

Specification	[8]	[7]	**This work**
Technology	16nm	40nm	**22nm FD-SOI**
Data Rate (Gbps)	56	20	**10**
Modulation	4-PAM	2-PAM	**2-PAM**
Type	Post-cursor	5-tap FFE	**Pre/post-cursor**
Power (mW)	34	26	**11**
Efficiency (pJ/bit)	0.6	1.3	**1.1**

B. PVT Compensation

To verify the PVT compensation strategy V_{dd} was increased by $+10$ %, and body bias voltages V_{bp} and V_{bn} were tuned to compensate for the higher transconductances. Shown in Fig. 8 is the equalizer's GD, measured for the nominal case (nom, $V_{dd} = 1$ V, $V_{bn} = 0.5$ V, and $V_{bp} = 0.5$ V), and compared against the uncompensated (uncomp, $V_{dd} = 1.1$ V, $V_{bn} = 0.5$ V, and $V_{bp} = 0.5$ V) and compensated (comp, $V_{dd} = 1.1$ V, $V_{bn} = 0$ V, and $V_{bp} = 1.1$ V) cases.

Table I summarizes recently published inverter-based CTLEs. The proposed precursor and postcursor equalizer consumes 11 mW from a typical 1-V supply (excluding the PGA and load matching, that are used for testing purposes only), resulting in a power efficiency of 1.1 pJ/b. While the implementation presented here is for the unique precursor and postcursor DWG channel characteristic, the technology, and technique shows promise for more complex wireline equalization with differentiated signal-to-noise advantages. This letter demonstrates a key element of single-chip SoC integrated DWG links, enabled by direct THz detection and transmission possible in 22-nm FD-SOI technology [9].

ACKNOWLEDGMENT

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REFERENCES

[1] J. Im *et al.*, "6.1 A 112 Gb/s PAM-4 long-reach wireline transceiver using a 36-way time-interleaved SAR-ADC and inverter-based RX analog front-end in 7 nm FinFET," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2020, pp. 1–2.

[2] S. Fukuda *et al.*, "A 12.5+12.5 Gb/s full-duplex plastic waveguide interconnect," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 3113–3125, Dec. 2011.

[3] P. Reynaert *et al.*, "Polymer microwave fiber: A new communication concept that blends wireless, wireline and optical communication," in *Proc. 26th IEEE Int. Conf. Electron. Circuits Syst. (ICECS)*, Nov. 2019, pp. 755–758.

[4] N. Dolatsha, C. Chen, and A. Arbabian, "Loss and dispersion limitations in mm-wave dielectric waveguides for high-speed links," *IEEE Trans. THz Sci. Technol.*, vol. 6, no. 4, pp. 637–640, Jul. 2016.

[5] M. De Wit, S. Ooms, B. Philippe, Y. Zhang, and P. Reynaert, "Polymer microwave fibers: A new approach that blends wireline, optical, and wireless communication," *IEEE Microw. Mag.*, vol. 21, no. 1, pp. 51–66, Jan. 2020.

[6] K. Ogusu, "Numerical analysis of the rectangular dielectric waveguide and its modifications," *IEEE Trans. Microw. Theory Techn.*, vol. 25, no. 11, pp. 874–885, Nov. 1977.

[7] R. Boesch, K. Zheng, and B. Murmann, "A 0.003 mm^2 5.2 mW/tap 20 GBd inductor-less 5-tap analog RX-FFE," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2016, pp. 1–2.

[8] K. Zheng *et al.*, "An inverter-based analog front-end for a 56-Gb/s PAM-4 wireline transceiver in 16-nm CMOS," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 12, pp. 249–252, Dec. 2018.

[9] R. Jain, R. Zatta, J. Grzyb, D. Harame, and U. R. Pfeiffer, "A terahertz direct detector in 22 nm FD-SOI CMOS," in *Proc. 13th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, 2018, pp. 25–28.