A 28-GHz, 18-dBm, 48% PAE Stacked-FET Power Amplifier with Coupled-Inductor Neutralization in 45-nm SOI CMOS

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***Abstract*—A single stage, millimeter-wave 2-stack FET power amplifier operates with a peak saturated power of 18.2 dBm and peak PAE of 48.2%. The high PAE results from a proposed C_{gd} neutralization through coupled inductor feedback between the drains of the stacked FETs. The technique reuses the interstage matching shunt inductor to reduce the loss and chip area while improving the PA gain. The PA achieves 13.6 dB gain with a 3 dB bandwidth of 12 GHz at a 2.4-V power supply. The PA is implemented in a 45-nm SOI CMOS technology using a trap-rich substrate and has an area of 520 μm $\times$ 530 μm. To the author's knowledge, this work demonstrates the highest gain and power added efficiency (PAE) for a single-stage Si-based PA at 28 GHz.**

***Index Terms*—28 GHz, Millimeter-wave, PA, Stacked FET, High Efficiency**

I. Introduction

A primary challenge for next-generation millimeter-wave wireless systems is highly efficient power amplifiers. Power amplifier (PA) efficiency imposes a power wall, particularly in arrays of transmitters. The past decade has seen significant progress in high-power and high-efficiency PAs at millimeter-wave bands. Stacked FET approaches offer higher output power due to the series voltage combining at the output [1], [2], [3]. High efficiency has been realized using class-E [4], inverse class-F [5] or tunable techniques based on a variant of inverse class-F [6]. At millimeter-wave bands, the gain of the transistor is quite low and the control of harmonics as demanded for class-E operation is difficult to achieve because it requires high order harmonics. Class-F or inverse class-F PA could shape the output current and voltage waveforms to reduce the DC power consumption on transistors, but it usually requires 2nd order and 3rd order harmonic tanks introducing loss. This work explores circuit improvements that result in better efficiency than earlier work while remaining in class-B.

This work proposes a circuit technique to neutralize the feedback capacitance, C_{gd}, in a stacked FET PA design. At high frequency, C_{gd} provides a feedback path that reduces the gain of the transistor while also reducing the output impedance. In a stacked-FET PA, the power is not efficiently combined due to the phase mismatch between V_{ds} and I_d introduced by the feedback capacitance. Earlier work recognized the importance of neutralization techniques to overcome the drawback of gate to drain capacitance. Here, we propose a coupled inductor neutralization for the stacked FET PA that is compact by reusing the interstage matching shunt inductor and output matching load inductor to reduce the number of passive components and loss.

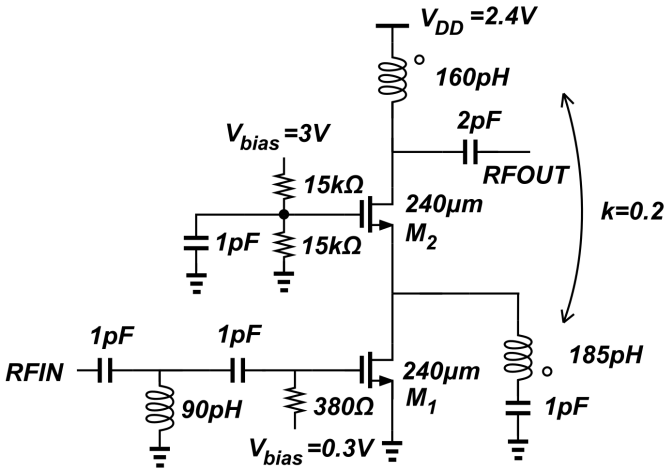


Fig. 1. Schematic of the transformer neutralization power amplifier

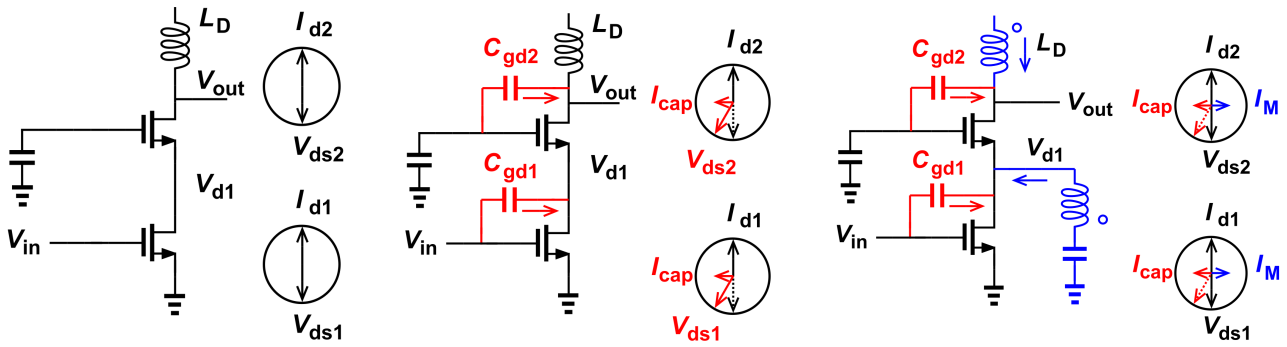
Section II describes the proposed PA and the transformer-based C_{gd} neutralization based on an analysis of the impact of C_{gd} at high frequency. In Section III, a 2-stack FET PA is presented that achieves wideband operation with high efficiency. Section IV presents the measurement results and demonstrates agreement with simulation results. A table of comparison illustrates the improvements to the state of art PA performance presented in this work. To author's knowledge, this work achieves highest PAE in CMOS, CMOS SOI and SiGe technology at 28 GHz.

II. Coupled-Inductor C_{gd} Neutralization

Fig. 1 shows the schematic of the 2-stack FET PA. The gate capacitor and C_{gs} of FET, M2, form a voltage divider which causes the voltage on the source, gate and drain of the transistor to remain in phase to reduce V_{gd} and allow efficient series power combining. The gate capacitor on the top FET is sized to ensure the voltage swing on V_{gd} less than 2.5V.

Fig. 2a shows the voltage and current phase at low frequency. Here, the impact of C_{gd} can be neglected and the V_{ds} is 180 degrees out of phase to I_d. By avoiding overlap between V_{ds} and I_d, the power dissipated across the FETs $P_{diss} = V_{ds}I_d$ is reduced and higher efficiency is achievable.

At high frequency, the efficiency of the stacked FET approach drops for two reasons. First, the gain of the stage is reduced and, second, the power dissipated by the devices increases due to the phase shift across devices in the stack. Fig. 2b shows the voltage and current phase change due to C_{gd}. A feedback current is injected through C_{gd} to the output



(a) Without C_{gd} (b) With C_{gd} (c) Coupled-inductor neutralization

Fig. 2. Effects of feedback through gate-drain capacitance and implementation of coupled-inductor neutralization

node because of the gate and drain voltage and induces a phase difference between I_d and V_{ds} such that the resulting V_{ds} is not 180 degree out of phase with I_d. Therefore, the output power of the stacked-FET PA reduces and P_{diss} increases for each FET.

Fig. 2c shows the proposed coupled-inductor neutralization. The interstage matching shunt inductor is coupled to the load inductor producing feedback to the interstage node. This coupling generates a mutual current on the drain node of both FETs that is 180 degree out of phase with current flowing through C_{gd}. The load inductor is chosen to tune out the output capacitance of the PA. The interstage inductor is chosen to resonate with drain capacitance of M1. Through appropriate choice of the coupling coefficient, the mutual current that negates the C_{gd} injection current. Increasing coupling coefficient should increase the output power as the total V_{ds} shifts out of phase with I_d. Additionally, the stability improves as the gate-drain capacitance is neutralized. We verify this in Fig. 3. Simulations indicate that as the coupling coefficient increases the PAE, increasing output power but then degrades as the gain reduces. The μ factor improves as well until the neutralization is over-compensated and the amplifier becomes unstable. This approach is robust because the optimal choice for the coupling coefficient in terms of PAE is well below the region that results in μ factor less than one. In this work, we use a coupling factor of k = 0.2. The coupled inductors are realized as two transmission lines on the top metal layer that are separated to weakly couple the lines.

III. Circuit Implementation

The coupled-inductor neutralized power amplifier was designed in a 45nm SOI CMOS process with 8 metal layers and trap-rich substrate. The top Aluminum metal layer is 4μm thick and is used for the signal line ground CPW transmission lines as well as inductors. EM simulations indicate the inductor quality factor with the trap-rich substrate exceeds 30 at 28 GHz.

In the 2-stack FET PA, M1 and M2 are floating body devices with a width of 240μm and 40-nm gate length. The NFET is modeled by PEX to include polysilicon and active region parasitics and routing up to the fourth metal layer while the

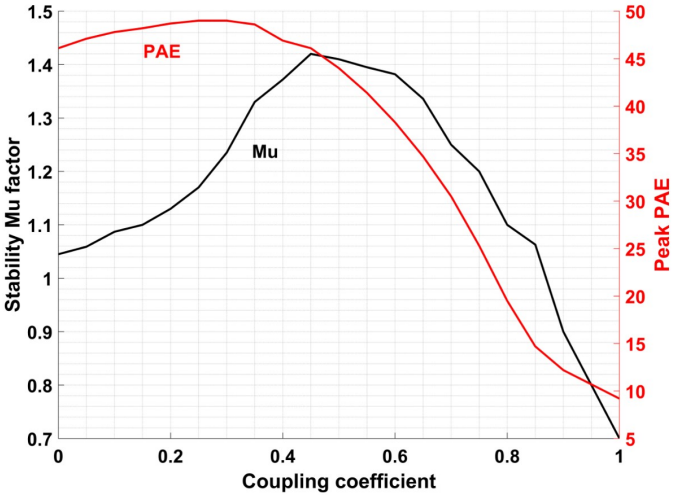


Fig. 3. Tradeoff between μ factor and PAE versus inductor coupling factor

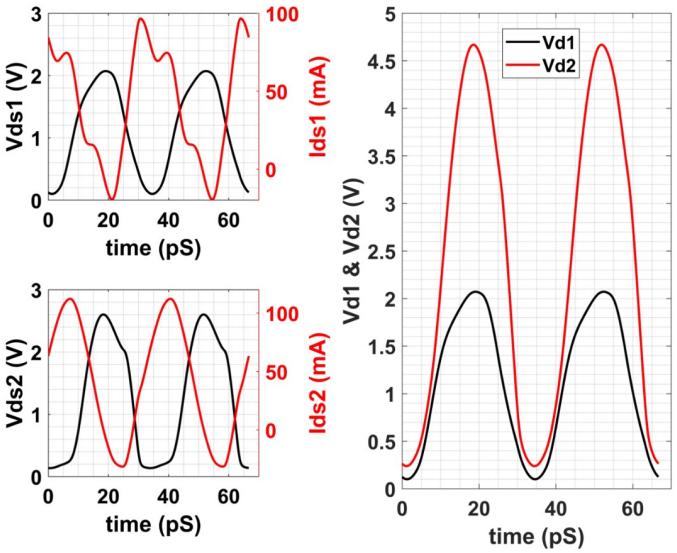


Fig. 4. Transient V_{ds} and I_d waveforms to illustrate the alignment of the drain source voltage to improve the output voltage swing

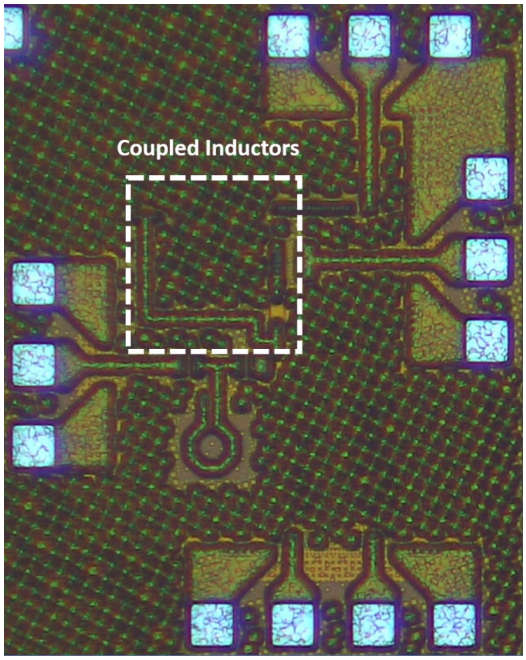


Fig. 5. Chip micrograph of the single stage of the 28 GHz PA

passive interconnections above the fourth layer were modeled by EMX. Each 240-μm wide NFET comprises two 120μm NFETs with 60 2μm wide fingers to reduce the gate resistance and phase difference between the fingers.

The transistor is biased in class B where the load line of each 240 μm NMOS is approximately 25 Ω. Consequently, two stacked FETs under class-B biasing exhibit a load line close to 50 Ω and the output matching network only tunes the C_{out} of the stack with a load inductor. DC blocking capacitors are included at the input and output of the amplifier to ease chip testing and provide a more accurate and complete comparison to earlier work. The gate capacitor of M2 is chosen to ensure the V_{gd} swing does not exceed 2.5V.

Simulations of V_{gs} and I_d for the M1 and M2 FETs are shown in Fig. 4. The phase of V_{ds1} and V_{ds2} are phase aligned to increase the output voltage swing.

IV. Measurement Results

Fig. 5 shows the chip micrograph. The PA area is 520 $\boldsymbol{\mu}$m $\times$ 530 $\boldsymbol{\mu}$m excluding pads. The PA has been measured using a Keysight N5247 PNA-X to 50 GHz. The simulated and measured $\boldsymbol{S}$-parameters of the PA are shown in Fig. 6. The measured results indicate excellent agreement with simulations. The peak gain is 13.6 dB at 30 GHz. The measured $\boldsymbol{S22}$ shifted 2 GHz higher and $\boldsymbol{S11}$ shifted 4 GHz lower in frequency. The circuit is unconditionally stable. The circuit illustrates wideband gain with a 3dB bandwidth from 25.5 to 37.5 GHz for a fractional bandwidth of 38%.

The PA achieves a peak saturated output power $\boldsymbol{P_{sat}}$ of 18 dBm and a peak PAE of 48.2% at 28 GHz. Fig. 7 shows the measured and simulated gain and PAE as a function of output power at 30 GHz. Notably, the efficiency is around

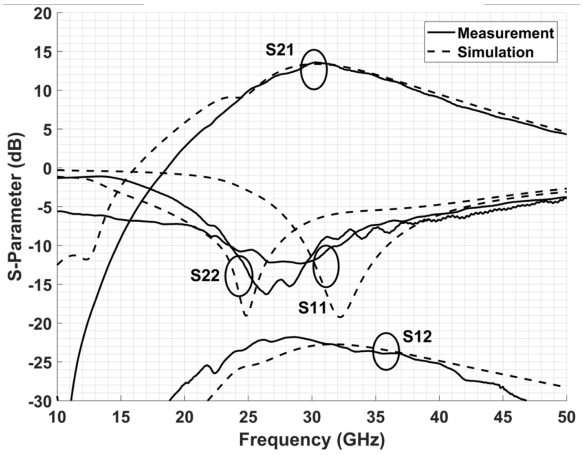


Fig. 6. S-parameter measurement and simulation comparison

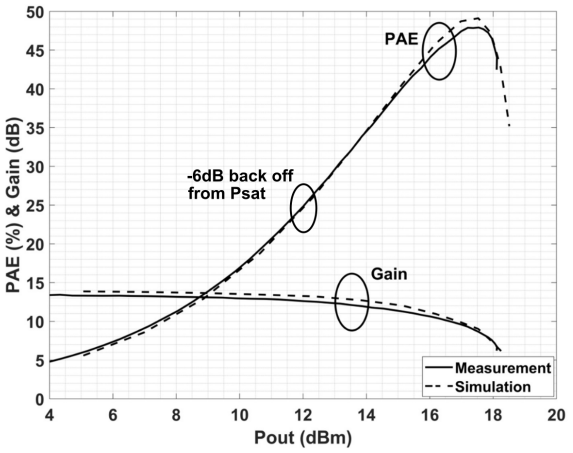


Fig. 7. PAE and gain versus output power at 30 GHz

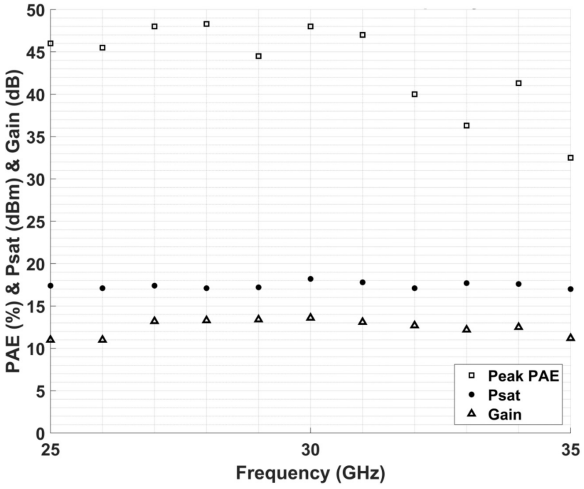
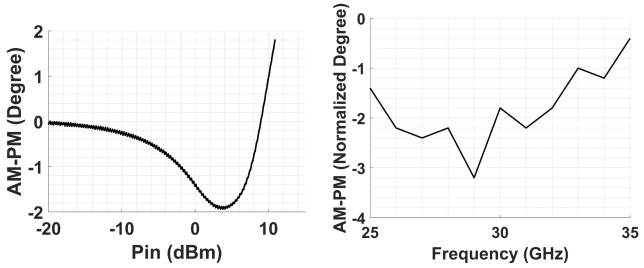


Fig. 8. Large signal measurement across the 3dB bandwidth

TABLE 1

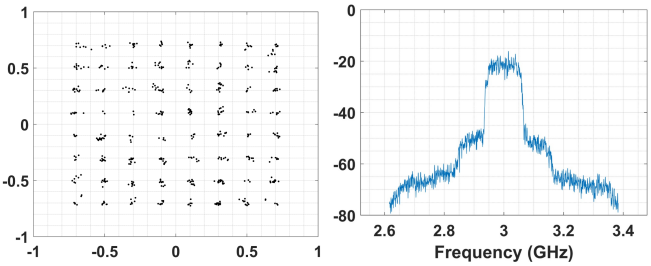
Param.\Ref.	[5]	[6]	[7]	[8]	[9]	**This work**
Tech CMOS	130nm SiGe	65nm	65nm	40nm	28nm	**45nm SOI**
Supply (V)	2.3	1.1	1.1	1	1.1	**2.4**
Frequency (GHz)	22-28	26-34	24-32	26-29	24-30	**25.5-37.5**
FBW (%)	24	26.7	28.6	10.9	22.2	**38**
P_{sat} (dBm)	18	14.75	15.6	18.1	19.8	**18**
P_{1dB} (dBm)	16	13.2	14	16.8	18.6	**16**
PAE at 28GHz (%)	36	44	41	41.5	41.4	**48.2**
Gain (dB)	21	10	15.8	20.5	13.6	**13.6**
Chip Size (mm^2)	0.6	0.12	0.24	0.36	0.28	**0.27**
FOM1	264	251	256	263	258	**258**

$FOM1(ITRS) = P_{sat} + Gain + 10log(PAE_{peak}) + 20log(Freq)$



(a) AM-PM vs Pin at 30 GHz (b) AM-PM vs Frequency at P_{1dB}

Fig. 9. AM-PM measurement



(a) 64QAM constellation with 100 MS/s (b) ACPR

Fig. 10. EVM measurement

24% at 6-dB back-off which matches expectations about class-B operation. Fig. 8 shows peak PAE, $\boldsymbol{P_{sat}}$ and gain of the proposed PA across the frequency band and indicates that high efficiency operation is achieved over a wide range of frequencies. The PAE is better than 45% from 25 to 31 GHz.

The AM-PM behavior of the PA is plotted in Fig. 9. The AM-PM variation indicates less than +/-2 degrees of variation at 30 GHz. Across the frequency band, the AM-PM variation is limited.

The excellent AM-AM and AM-PM behaviors are illustrated by the filtered 64-QAM constellation in Fig. 10 with a PAPR of 6 dB. The 64-QAM constellation exhibits an EVM of 4.2% at an output power of 8.4 dBm without the use of predistortion. The ACPR is shown in Fig. 10b.

Table I compares the performance of this work with recently published results in CMOS, CMOS SOI and SiGe HBT technologies. To the best of our knowledge, this PA presents record PAE at 28 GHz of 48.2% for a Silicon process. Additionally, the fractional bandwidth and gain of the stage are excellent.

V. Conclusion

A single-stage 2-stack FET power amplifier is presented using a proposed coupled inductor $\boldsymbol{C_{gd}}$ neutralization to adjust the phase between the drain-source voltage across the stacked FET transistors. The measurement results show excellent agreement with the simulation results and demonstrate a peak PAE of 48.2% at 28 GHz and output power of 18 dBm.

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References

[1] B. Hanafi, O. Grbz, H. Dabag, J. F. Buckwalter, G. Rebeiz, and P. Asbeck, "$\boldsymbol{Q}$-Band Spatially Combined Power Amplifier Arrays in 45-nm CMOS SOI," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 6, pp. 1937–1950, June 2015.

[2] J. A. Jayamon, J. F. Buckwalter, and P. M. Asbeck, "Multigate-Cell Stacked FET Design for Millimeter-Wave CMOS Power Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 9, pp. 2027–2039, Sept 2016.

[3] H. T. Dabag, B. Hanafi, F. Golcuk, A. Agah, J. F. Buckwalter, and P. M. Asbeck, "Analysis and Design of Stacked-FET Millimeter-Wave Power Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 4, pp. 1543–1556, April 2013.

[4] A. Chakrabarti and H. Krishnaswamy, "High-Power High-Efficiency Class-E-Like Stacked mmWave PAs in SOI and Bulk CMOS: Theory and Implementation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 8, pp. 1686–1704, Aug 2014.

[5] S. Y. Mortazavi and K. J. Koh, "Integrated Inverse Class-F Silicon Power Amplifiers for High Power Efficiency at Microwave and mm-Wave," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 10, pp. 2420–2434, Oct 2016.

[6] S. N. Ali, P. Agarwal, S. Mirabbasi, and D. Heo, "A 42-46.4% PAE continuous class-F power amplifier with Cgd neutralization at 26-34 GHz in 65 nm CMOS for 5G applications," *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2017, pp. 212–215.

[7] S. N. Ali, P. Agarwal, J. Baylon, S. Gopal, L. Renaud, and D. Heo, "A 28GHz 41%-PAE linear CMOS power amplifier using a transformer-based AM-PM distortion-correction technique for 5G phased arrays," in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, Feb 2018, pp. 406–408.

[8] Y. Zhang and P. Reynaert, "A high-efficiency linear power amplifier for 28GHz mobile communications in 40nm CMOS," in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2017, pp. 33–36.

[9] B. Park, S. Jin, D. Jeong, J. Kim, Y. Cho, K. Moon, and B. Kim, "Highly Linear mm-Wave CMOS Power Amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 12, pp. 4535–4544, Dec 2016.