A 30-GHz CMOS SOI Outphasing Power Amplifier With Current Mode Combining for High Backoff Efficiency and Constant Envelope Operation

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***Abstract*— High peak and average efficiency is an important feature of power amplifiers (PAs) for 5G millimeter-wave communication. This article reviews the challenges of conventional outphasing approaches in CMOS technologies and demonstrates a low-loss outphasing combiner for low loadline impedance. Undesirable characteristics of CMOS devices for outphasing are compensated with neutralization, unilaterization, and stabilization networks for the outphasing PA (OPA). The OPA is realized in 45-nm CMOS silicon on insulator (SOI) and demonstrates 40% 6-dB backoff drain efficiency (DE) while providing 17-dBm peak output power with a peak 50.5% DE. For 64-QAM, a 31.3% average DE and 10.1-dBm average output power are measured. The OPA demonstrates less than 1.5% error vector magnitude (EVM) with 64-QAM waveform using a phase-based lookup table (LUT). With 16-QAM, the bit rate reaches 20 Gb/s with 12% EVM. To the best of our knowledge, this is the highest bit rate for a high-efficiency PA. The adjacent channel leakage ratio (ACLR) is under −25 dBc.**

***Index Terms*— 5G, Chireix power combiner, millimeter wave (mm-wave), outphasing power amplifier (OPA), power amplifier (PA), silicon on insulator (SOI) CMOS.**

I. Introduction

THE emerging focus on fifth-generation (5G) wireless communication is developing millimeter-wave (mm-wave) technology compatible with silicon-based CMOS process technologies. Transmitters designed for the 28-GHz band will support cyclic-prefix orthogonal frequency-division multiple access (CP-OFDMA) and QAM waveforms, potentially with multiple beams, pushing requirements on high peak-to-average power ratio (PAPR) above 10 dB. Additionally, high rates up to 20 Gb/s are proposed over 2-GHz channel bands, but ACLR is relaxed to −17 dBc compared to earlier 4G LTE [1]. A key research challenge is to demonstrate CMOS power amplifiers (PAs) at 28 GHz with higher average efficiency at 6- or 10-dB output backoff (OBO) power levels. [2]–[8].

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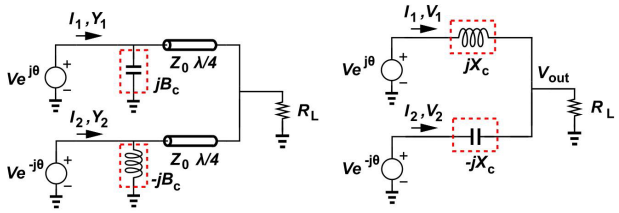

Fig. 1. Conventional OPA with voltage-mode PAs and voltage-mode power combiner (left) and proposed OPA with voltage-mode PAs and current-mode power combiner (right).

To address high PAPR, conventional approaches for mm-wave PAs include envelope tracking, Doherty, and OPAs [9], while popular for RF bands, the efficiency of supply modulators drops rapidly at gigahertz envelope bandwidths, resulting in low average efficiency and difficulty in operating with arrays [10]–[12]. Load modulation techniques, including Doherty and outphasing, are promising but are also confronted by significant challenges when realized with silicon CMOS processes. Several Doherty PAs have been proposed recently to provide OBO drain efficiency (DE) (η) improvement but require significant analog or digital predistortion (DPD) and lossy power combiners [13]–[19]. DPD becomes difficult to realize in beamformers when per-element observation is required to correct for gain variation. Recent work [20] has shown that calibrating the outphasing signals is energy efficient and practical since it requires timing precision at baseband.

Outphasing power amplifiers (OPAs), on the other hand, tend to suffer from lossy power combiners but have the advantage of using constant envelope signaling. The outphasing PA operates in class-B at mm-wave bands to realize the highest gain, and a conventional Chireix power combiner requires two quarter-wavelength transmission lines in the power combiner, as shown in Fig. 1. In [21], a triaxial balun is proposed as the outphasing combiner using a sub-quarter-wavelength balun [22] to reduce the combiner loss to around 0.5 dB. However, this low-loss triaxial balun design is not easily realized in the CMOS processes due to the proximity of the metal layers to the ground and the lower loadline impedance of the CMOS device. Series combiners have been proposed at RF bands [23]–[25]. Here, we demonstrate an mm-wave series combiner as shown in Fig. 1 to improve the class-B waveform behavior over OBO conditions with lower loss. While earlier work on

OPAs required non-constant amplitude and outphasing angle variation for high efficiency [26]–[28], we demonstrate that the current-mode combiner allows true constant envelope signals to realize high average efficiency.

This article proposes a low-loss current-mode power combiner for the OPA appropriate for the characteristics of a silicon CMOS process. Section II reviews the conventional Chireix OPA and details of the limitations in mm-wave bands. In Section III, a current-mode combiner is presented and the impact of parasitics that strongly degrade CMOS PAs at mm-wave bands, particularly $C_{\rm gd}$ and $C_{\rm ds}$, on η at OBO levels are detailed. Section IV describes the mm-wave PA circuit-level simulations, including neutralization, unilaterization, and stabilization techniques to improve the average efficiency. Finally, we demonstrate true constant envelope waveform generation and linearization to realize low error vector magnitude (EVM) with high-order QAM at 30 GHz and compare to the state of the art in Section V.

II. Outphasing Power Combiners

Chireix introduced the OPA in 1935 and recent work has shown that this approach can be adapted to mm-wave bands [29]. In the conventional OPA, a complex RF signal is decomposed into two constant envelope signals that are separated by an outphasing angle θ, while the common-mode phase of the two signals is the phase modulation ϕ.

As shown in Fig. 1, two voltage-mode outphasing signals $Ve^{j\theta}$ and $Ve^{-j\theta}$ are combined through two $\lambda/4$ transmission lines with characteristic impedance Z_0. The output power varies with the outphasing angle θ, and the admittances seen at the output of the amplifiers ($k = 1$ and 2) are

$$Y_k = \frac{I_k}{V_k} = \frac{2\cos^2\theta}{R'_L} \mp j\frac{\sin 2\theta}{R'_L} = G_0 \mp jB_0 \tag{1}$$

where $R'_L = (Z_0^2/R_L)$. The RF output power and DC power consumed at the drain of each PA are

$$P_{{\rm RF},k} = \frac{1}{2}{\rm Re}\left(V_k^* Y_k^* V_k\right) = \frac{1}{2}|V_k|^2 G_0 \tag{2a}$$

$$P_{{\rm DC},k} = I_{\rm DC}V_{\rm DC} = \frac{2}{\pi}\left|V_k^* Y_k^* V_k\right| = \frac{2}{\pi}|V_k|^2|Y| \tag{2b}$$

where the maximum amplitude $|V_k|$ is $V_{\rm DC}$ based on class-B PA output voltage waveform assumption and ignoring the knee voltage. We note that $P_{\rm RF}$ is proportional to G_0 and $P_{\rm DC}$ is proportional to $(G_0^2 + B_0^2)^{1/2}$. Therefore, the DE of the PA is

$$\eta_{\rm VM} = \frac{P_{\rm RF}}{P_{\rm DC}} = \frac{\pi}{4}\frac{G_0}{\sqrt{G_0^2 + B_0^2}}. \tag{3}$$

The OPA η reaches a maximum class-B peak efficiency (78%) when the susceptance is zero.

To control the range over which the OPA η is high under backoff conditions, the compensating susceptance $\pm B_C$ is introduced in the conventional Chireix power combiner as shown in Fig. 1 to drop $P_{\rm DC}$ more quickly than the output power $P_{\rm RF}$. The admittance seen looking into the two paths becomes

$$Y_k = G_0 \mp j(B_0 - B_C). \tag{4}$$

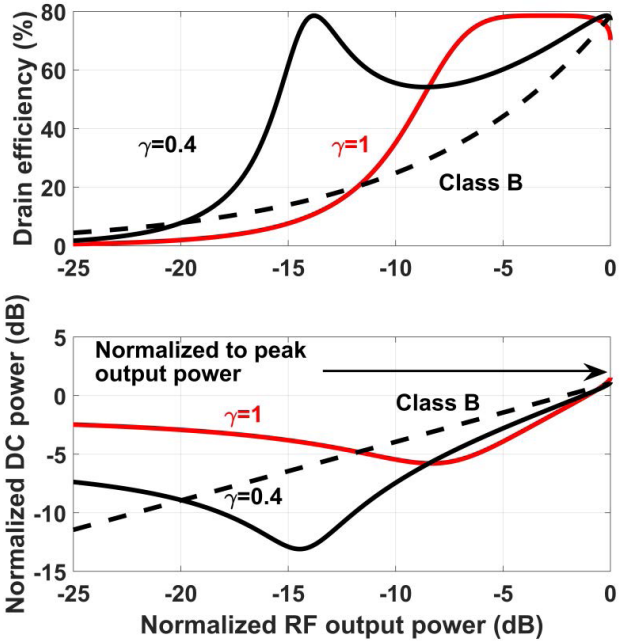

Fig. 2. Conventional DE and DC power consumption for OBO power levels.

In the presence of $\pm B_C$, $P_{\rm DC}$ drops as shown in Fig. 2 as η under OBO is improved. Based on the choice of B_C, η peaks at different backoff power levels. If $B_C = \gamma B_0$, η for voltage-mode sources is expressed as

$$\eta_{\rm VM} = \frac{P_{\rm RF}}{P_{\rm DC}} = \frac{\pi}{4}\frac{G_0}{\sqrt{G_0^2 + B_0^2(1-\gamma)^2}}. \tag{5}$$

A key insight into the operation of the Chireix combiner is that the DC power is controlled to improve efficiency under OBO conditions, while in Doherty amplifiers, the delivered output power is controlled by the auxiliary amplifier. As shown in Fig. 2, the minimum $P_{\rm DC}$ occurs at lower $P_{\rm RF}$ and the smaller coefficient ($\gamma = 0.4$) provides more DC power reduction.

The reflection coefficients seen at the output of the PAs in the presence of B_C are shown in Fig. 3 as a function of outphasing angle. The real part of the impedance changes from 25 to 500 Ω limiting the output power and efficiency that are achievable in CMOS technology.

Unfortunately, other factors also limit the conventional Chireix combiner in mm-wave frequency bands. The intrinsic transistor parasitics, such as $C_{\rm ds}$ and $C_{\rm gd}$ shown in Fig. 4, impact the PA efficiency in mm-wave bands by shifting the desired loadline impedance.

If the PA includes a significant output capacitance comprising $C_{\rm ds}$ and $C_{\rm gd}$, the contribution of the output capacitance is defined by $\alpha B_0 = \omega C_{\rm out}$, and the efficiency becomes

$$\eta_{\rm VM} = \frac{\pi}{2}\frac{1}{\sqrt{1 + \frac{B_0^2}{G_0^2}(1-\gamma-\alpha)^2} + \sqrt{1 + \frac{B_0^2}{G_0^2}(1-\gamma+\alpha)^2}}. \tag{6}$$

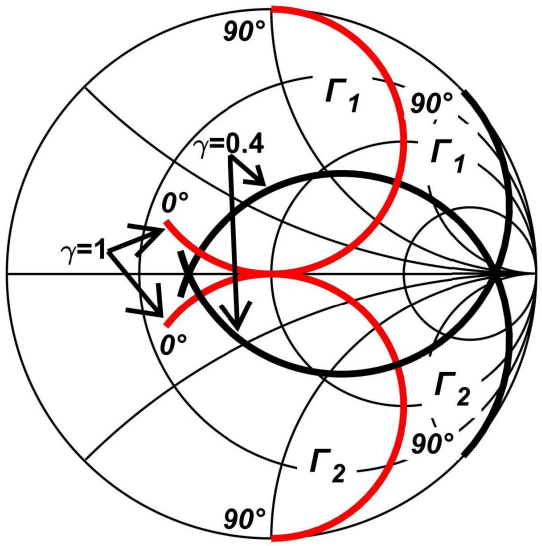

Fig. 3. Smith chart illustrating the reflection for Chireix combiner for different values of γ with sweeping the outphasing angle from 0° to 90°.

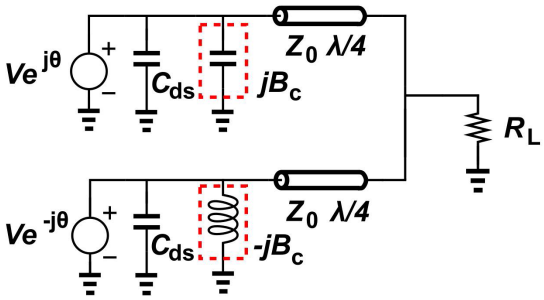

Fig. 4. Role of transistor output capacitance in Chireix combiner.

If we choose $Z_0 = 50\ \Omega$ and $\gamma = 0.4$ at 30 GHz for the Chireix combiner, the combiner is compensated with a capacitor of 42 fF. In a 45-nm CMOS process, a transistor that is capable of delivering a peak power of 16 dBm has a $C_{\rm ds}$ of around 50 fF. While some of the output capacitance can be incorporated into the Chireix compensation capacitance, Fig. 5 shows that 20 fF causes η to drop to 56% from 78% peak at the 6-dB OBO power. At this point, the advantage over a class-B PA is greatly diminished.

Since $C_{\rm gd}$ changes the phase between the output voltage and current waveforms, it also tends to contribute to a degradation in gain and efficiency under OBO conditions. The voltage difference between the gate and drain changes with outphasing angle, and the current between the gate and drain, $I_{\rm gd}$, also changes, causing the output drain voltage to overlap the drain current and the efficiency drops [30], [31].

Additionally, $C_{\rm gd}$ varies the transistor output capacitance making it difficult to absorb the output capacitance into the Chireix combiner. Small-signal intuition suggests that the feedback capacitance generates a gain-dependent output capacitance, $C_{\rm out} = C_{\rm ds} + (1 + (1/A_v))C_{\rm gd}$. This is close to $C_{\rm gd}$ if the voltage gain A_v is high, but the gain is limited in mm-wave bands and changes with θ. Therefore, the impact of $C_{\rm gd}$ is to produce a contribution to α from (6) that changes with θ.

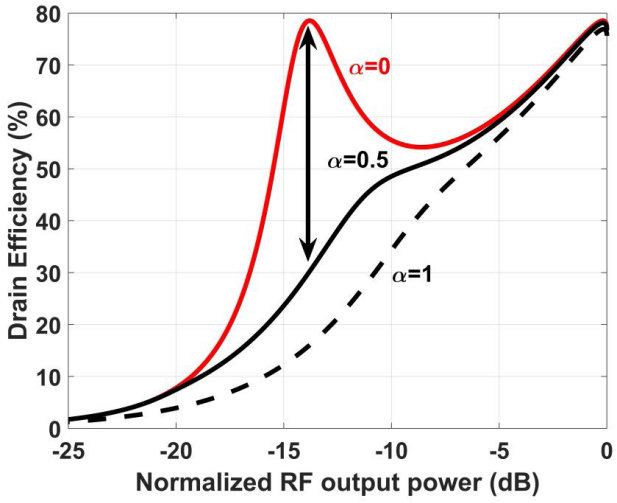

Fig. 5. Efficiency drops under backoff conditions for $\alpha = 0$ ($C_{\rm out} = 0$), $\alpha = 0.5$ ($C_{\rm out} = 21$ fF), and $\alpha = 1$ ($C_{\rm out} = 42$ fF) when $\gamma = 0.4$.

For this reason, unilaterization techniques, such as cross-coupled capacitors, offer limited efficiency improvement under OBO conditions for mm-wave OPAs [32].

III. Hybrid-Mode Outphasing Power Combining

The previous discussion presented the limitations of a Chireix outphasing power combining in mm-wave bands. Fundamentally, the Chireix combiner is presented as a voltage-mode combiner, driven with two voltage sources. Earlier work at RF bands explores the approach shown in Fig. 1 and combines the features of a voltage-mode PA with a current-mode power combiner [23]–[25]. Here, we investigate the hybrid-mode operation by considering a series (current mode) combining with a voltage-mode PA. To maintain constant envelope signaling, the condition for the hybrid-mode outphasing operation satisfies

$$V_{\rm out} - V e^{\pm j\theta} = \mp j X_C I_{1,2}. \tag{7}$$

Solving for I_1, I_2, and $V_{\rm out}$, the output voltage is

$$V_{\rm out} = 2V \frac{R_L}{X_C} \sin\theta. \tag{8}$$

Now, the output voltage depends on the compensation reactance X_C and is suitable for CMOS PAs where low loadline impedance is typical for high output power. The output currents are

$$I_k = V \frac{\sin\theta}{X_C} \mp jV \left(\frac{\cos\theta}{X_C} - \frac{2R_L \sin\theta}{X_C^2} \right). \tag{9}$$

The admittance seen looking into the combiner is

$$Y_k = \frac{I_k}{V_k} = 2\sin^2\theta \frac{X_C^2}{R_L} \mp j \left(\frac{1}{X_C} - \sin 2\theta \frac{X_C^2}{R_L} \right). \tag{10}$$

Therefore, the RF output power and DC power consumption are

$$P_{\rm RF} = \frac{1}{2}|V|^2 Re\{Y_1^*\} = |V|^2 \sin^2\theta \frac{R_L}{X_C^2} \tag{11a}$$

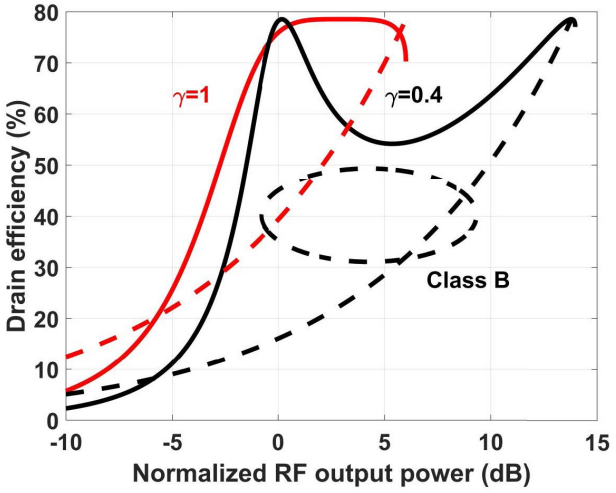

Fig. 6. DE for the current-mode combiner for different compensation coefficients. The plot is normalized for the minimum P_{DC}.

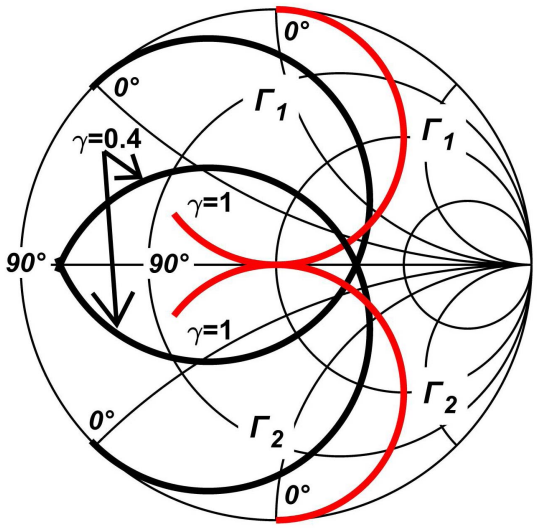

Fig. 7. Smith chart illustrating the impedance variation seen at the output of the two PAs for the current-mode combiner.

and

$$P_{\mathrm{DC}} = \frac{2}{\pi}|V|^2\frac{R_L}{X_C^2}\sqrt{(2\sin^2\theta)^2 + \left(\frac{X_C}{R_L} - \sin 2\theta\right)^2}. \quad (11b)$$

Consequently, the current-mode OPA output power exhibits different backoff characteristics when compared with the voltage-mode Chireix OPA. Comparing (2a) with (11b) demonstrates that the RF power is now modulated by the outphasing angle and the output power from current-mode OPA is related to the compensation component X_C. η_H is given by

$$\eta_H = \frac{\pi}{2}\frac{\sin^2\theta}{\sqrt{4\sin^4\theta + \left(\sin 2\theta - \frac{X_C}{R_L}\right)^2}}. \quad (12)$$

The peak efficiency is controlled by the ratio (X_C/R_L), and when this ratio equals to $\sin 2\theta$, it provides the same efficiency curve as (5); however, the output power is also related to X_C. Smaller X_C reaches higher peak output power, as shown in Fig. 6. For instance, the peak efficiency at 14-dB OBO occurs when $\theta = 80$ for $\gamma = 0.4$. As in voltage-mode power combiner topology, $\gamma = 1$ presents resistance between the two paths. $\gamma = 0.4$ suggests that the reactances are partially compensated by the series inductor and capacitor.

Most notably, the benefit of the current-mode combiner is shown in Fig. 7. The impedances that are required for high average efficiency are shifted to much lower loadlines that are compatible with CMOS devices.

When we review the role of C_{out} in the current-mode combiner, the DE illustrates less sensitivity to the role of parasitic shunt capacitance as we observed for the Chireix combiner. For C_{ds} of 20 fF, the OBO efficiency peak drops only 10% and still offers significant advantages compared with a Chireix combiner shown in Fig. 5. Since it obviates the need for quarter-wave transmission lines as shown in Fig. 1, a lower loss combiner may also be possible and will be investigated in Section IV.

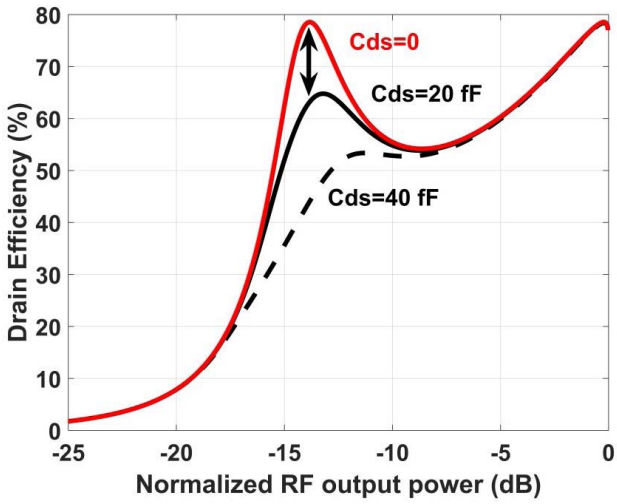

Fig. 8. Efficiency degradation across backoff conditions for $C_{\mathrm{ds}} = 0$, $C_{\mathrm{ds}} = 21$ fF, and $C_{\mathrm{ds}} = 42$ fF for hybrid power combiner for γ of 0.4.

To compare the voltage- and current-mode Chireix combiners, we plot the change in the load impedance presented to the outphasing PAs in the presence of a 40-fF output capacitance, e.g., C_ds, in Figs. 8 and 9. This variation is anticipated to be the result of process and modeling variation. Notably, the current-mode combiner impedance is shifted only slightly with respect to the ideal curves shown in Fig. 7. On the other hand, the voltage-mode combiner impedance is rotated substantially compared to Fig. 3 and results in much lower efficiency relative to the optimal loadline matching. The impedance shift causes the efficiency to drop at back off, as illustrated in Figs. 5 and 8. From this simulation, we find that the current-mode combiner is more robust to output capacitance changes.

IV. 28-GHz Silicon On Insulator (SOI) CMOS Outphasing PA Design

The schematic of the proposed hybrid-mode OPA is shown in Fig. 10, where each PA consists of a single common-source

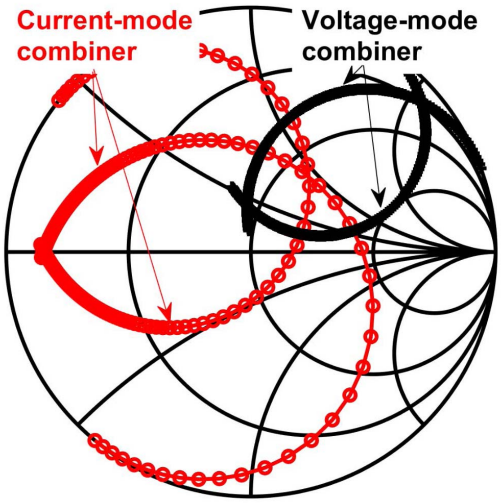

Fig. 9. Impedance variation with 40-fF C_{ds} in voltage-and current-mode power combiner.

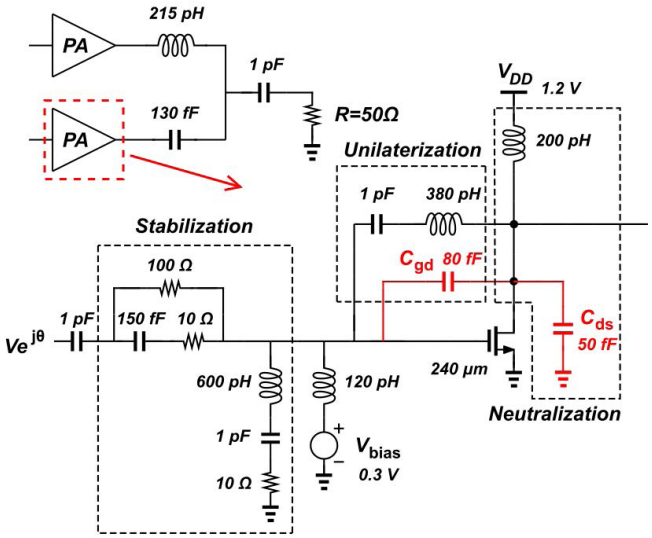

Fig. 10. Schematic of the proposed OPA with the neutralization, unilateralization, and stabilization networks.

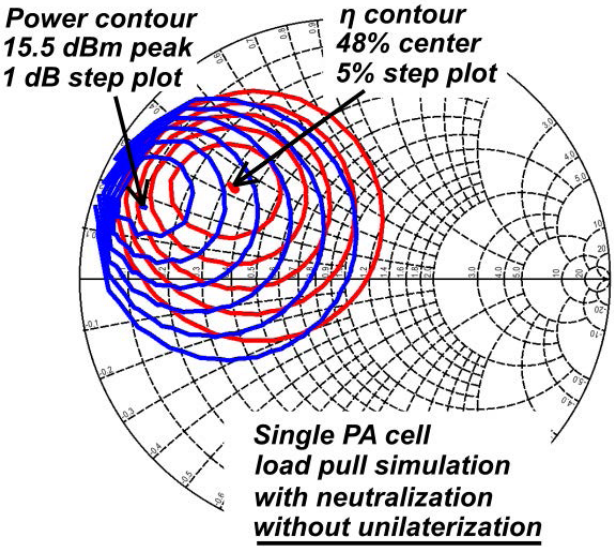

Fig. 11. Load-pull simulation of PA cell without unilaterization.

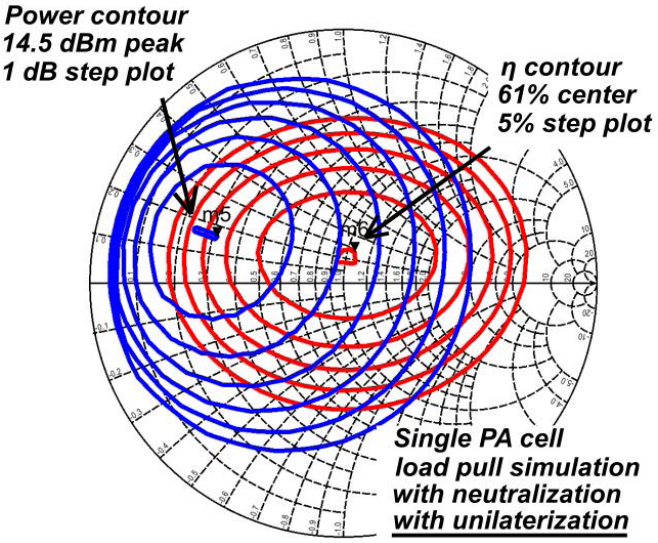

Fig. 12. Load-pull simulation of PA cell with unilaterization.

NMOS FET (NFET) biased in class B. The OPA is designed in GlobalFoundries 45RF SOI CMOS process and includes a pair of identical PA stages combined with the described current-mode power combiner. A 240-μm-wide NFET produces a load-line impedance close to 25 Ω when delivering 15 dBm of output power. Because the PA loadline is small relative to 50 Ω, the real part of the load impedance seen in the two paths ranges from 25 to 50 Ω.

A. PA Design

The PA circuit design consists of three key design components to realize high average efficiency: a neutralization network to compensate the reactance of C_{ds} that degrades backoff efficiency, a unilaterization network to minimize the current feedback through C_{gd} to improve load modulation, and a stabilization network to compensate the impact of the unilateralization and neutralization networks on the PA stability.

The load inductor is chosen to neutralize all the parasitic capacitance on drain node, including C_{ds}, parasitic capacitance from power combiner, and inductor load. A 200-pH inductor is used to resonate with the output capacitance of the 240-μm transistor. The NFET is unilaterized with a 380-pH inductor in series with a 1-pF DC blocking capacitor connected between the gate and drain to resonate out C_{gd} near 28 GHz. It should be noted that this network provides a feedback path at low frequency, near 6 GHz and impacts the circuit stability at lower frequencies.

Figs. 11 and 12 show the benefit of the neutralization and unilaterization networks for compensating C_{ds} and C_{gd}. Without unilaterization, the peak DE is 48% and the peak power is 15.5 dBm. Furthermore, η drops to 24% at the 6-dB OBO, half of its the peak value eliminating any advantage to outphasing relative to a class-B PA.

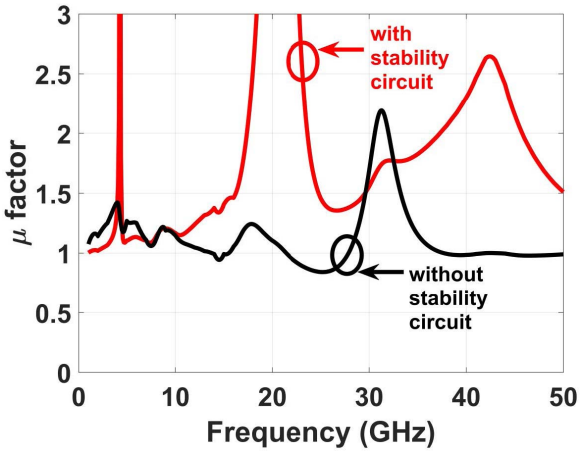

Fig. 13. Simulated μ factor of a single PA cell with and without the input high-pass network.

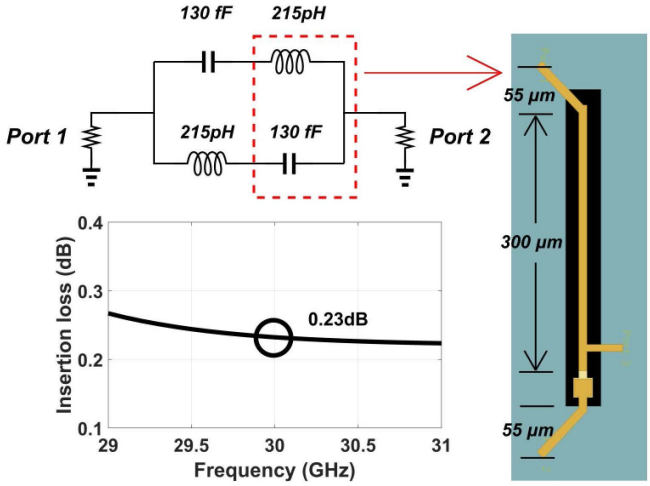

Fig. 14. Simulated insertion loss of the outphasing power combiner.

With the C_{gd} unilaterization, the peak η increases to 61%, while the output power drops to 14.5 dBm. Now, η drops to 51% at 6-dB OBO, significantly higher than half of its peak value (30%).

The introduction of the unilateralization network introduces conditional stability at other frequencies. A shunt low-frequency trap is designed at the gate using a 600-pH inductor in series with a 1-pF capacitor and a 10-Ω resistor to provide low impedance near 6 GHz and marked as stabilization in Fig. 10 [33]. Fig. 13 shows the source stability factor over a broadband with the low-frequency trap. Notably, the PA is not unconditionally stable below 28 GHz. To further improve the stability of the PA cell, a high-pass circuit input network reduces the reflection at the gate to ensure that a single PA cell is unconditionally stable. The μ factor of each PA is shown to be unconditionally stable in Fig. 13.

B. Combiner Design

The choice of the series reactance, X_C, in the current combiner provides different OBO power ranges. The compensation coefficient, $\gamma = 0.4$, is chosen based on producing a real part of the impedance seen into the two paths that are in the range of 25–50 Ω. Based on $X_C = \gamma X_0$, a 215-pH series inductor and a 130-fF series capacitor are added on the two paths.

The inductor uses a 4-μm-thick, 10-μm-wide metal to improve the quality factor (Q). The process offers a high-Q (>100) MIM capacitor for the combiner. The capacitor has been simulated with EM software EMX to verify the quality factor. The current combiner is simulated with a back-to-back configuration as shown in Fig. 14 and indicates that the total loss of the power combiner is 0.23 dB at 30 GHz. The layout of the current combiner is shown aside in the plot and illustrates the compact implementation of the outphasing combiner.

C. Dependence on VSWR

To investigate the sensitivity of the hybrid-mode OPA to load variations at the antenna, the output of the OPA was subjected to load pull at the output to assess the DE degradation at 6-dB OBO. As plotted in Fig. 15, the simulated η plots 2% contour drops in the efficiency for different load impedances. While η peaks at 54.5% around 35 Ω, η reduces to 52.5% for load resistances between 25 and 50 Ω.

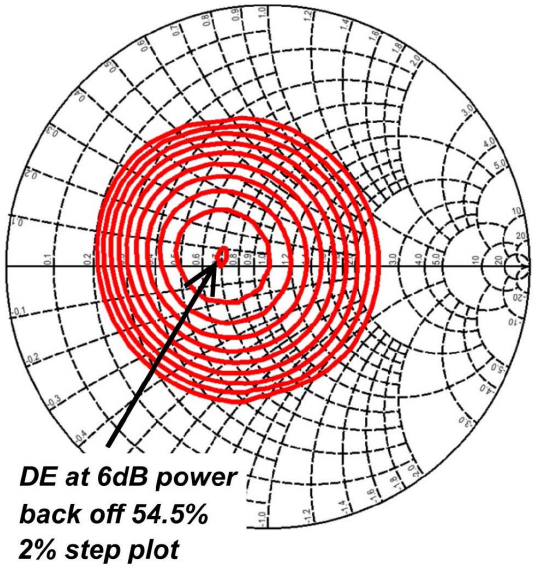

Fig. 15. Simulated η contour at 6-dB OBO from the peak output power ($\theta = 20°$).

V. Outphasing PA Measurement

Fig. 16 shows the chip microphotograph of the proposed OPA implemented in the GlobalFoundries 45-nm CMOS SOI process. The chip size is 920 μm × 1790 μm, including bondpads. The PAs are supplied with a 1.2-V voltage supply, and the gates are biased at 0.3 V for class-B operation.

A. Small-Signal Characterization

Since the outphasing PA is a three-port network with two input ports and a single output port, the measured S-parameters are compared to simulated S-parameters by sequentially measuring each PA. The measured results in Fig. 17 match the

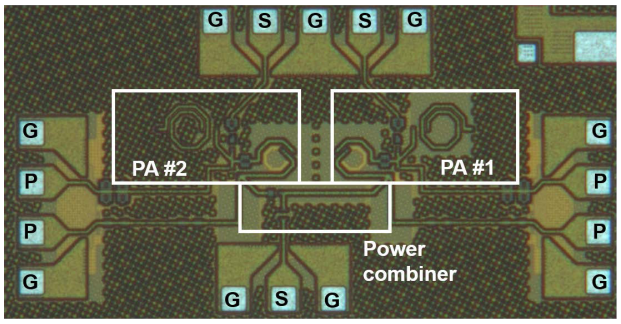

Fig. 16. Micrograph of the hybrid-mode OPA chip.

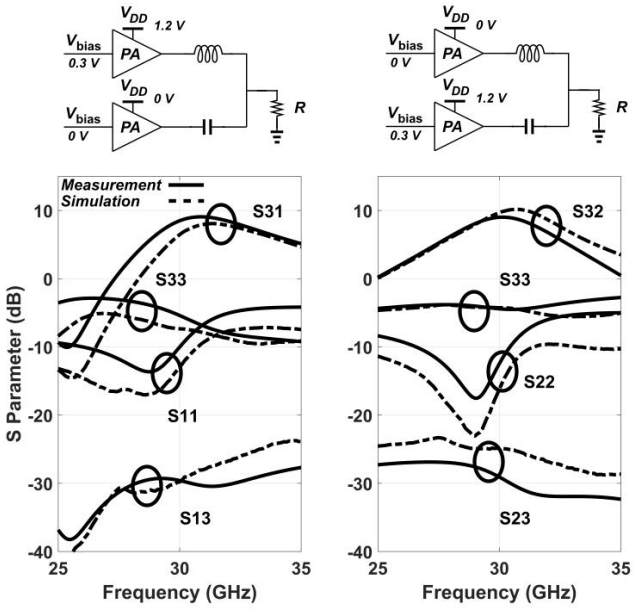

Fig. 17. Measured S-parameters for a single PA cell compared to simulations.

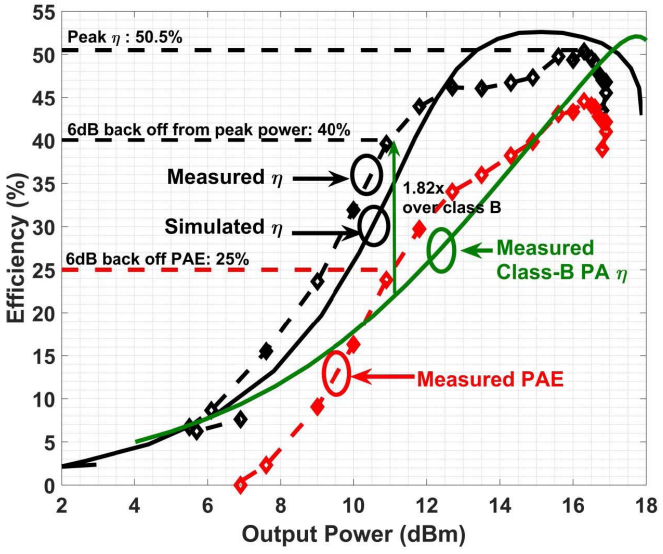

Fig. 18. Measured efficiency result comparing with simulation.

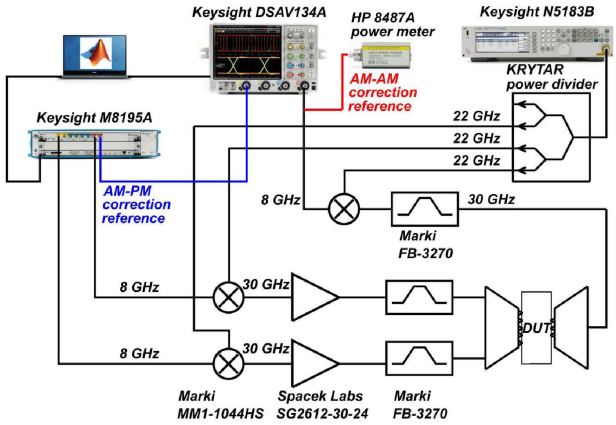

Fig. 19. Measurement setup.

simulation results accurately. Under these conditions, the PAs are unconditionally stable and simulated single PA μ factor is plotted in Fig. 13.

B. CW Power Measurement

The phase to each of the OPA inputs is calibrated and de-skewed to ensure that the input signals have the correct outphasing angle. Two signals generated by the AWG are shorted from input to output probe separately and compared to an 8-GHz reference generated from the AWG to calibrate the phase mismatch. After calibration, the phase mismatch from the AWG to the input probe is calculated and compensated in the output waveform of the AWG. In continuous-wave (CW) measurements for η and power added efficiency (PAE), the output probe connects to the power meter.

The outphasing angle θ is swept and the output power is recorded. As shown in Fig. 18, the measured peak output power of outphasing PA is 17 dBm at 30 GHz with 50.5% peak η. The peak PAE is 45% at 16.2-dBm output power. At 6-dB OBO, η is 40%, while PAE is 25%. The simulated voltage-mode PA with voltage-mode power combiner has a similar peak η but at 6-dB OBO, the η drops to 32%, much lower than η presented in current-mode power combiner. However, to the best of our knowledge, this is the highest efficiency at 6-dB OBO for a CMOS PA in this band. We attribute some η degradation to the VSWR of the power meter (1.4), which presents a 50-Ω measurement plane at the output of the OPA.

We compare the DE of the OPA to a neutralized class-B PA from our previous work [31] where the PA has 18-dBm peak output power with −28-dBc adjacent channel power ratio (ACPR), which is close to the OPA in terms of output power and linearity. The 6-dB OBO DE is less than 25% and is around 15% lower than the DE for the measured OPA.

C. Memoryless Outphasing AM–AM/AM–PM Compensation

The chip is measured on wafer using the test setup shown in Fig. 19 to characterize the outphasing performance. The signal generation and phase calibration are performed offline in MATLAB, and a waveform is downloaded to a Keysight M8195A AWG as a pair of constant envelope IF outphasing signals at 8 GHz. The IF signals are upconverted to

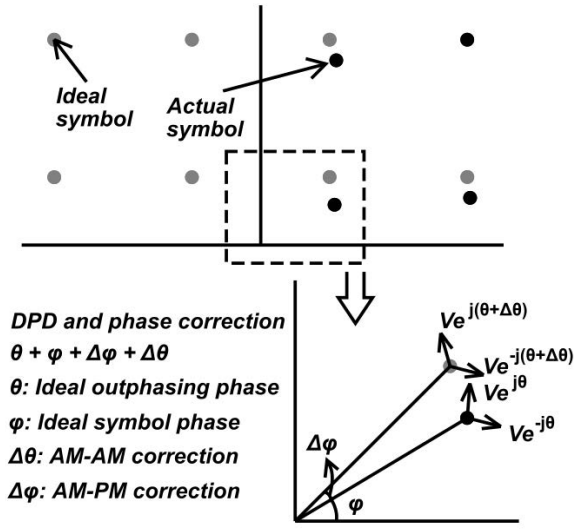

Fig. 20. Theory of phase-only DPD.

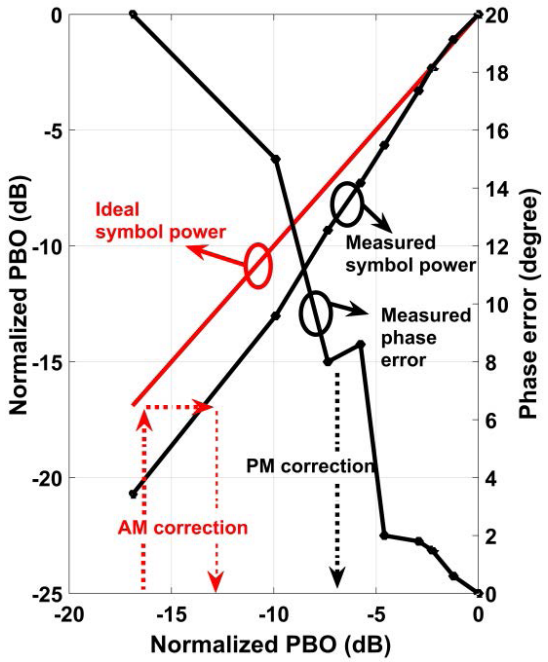

Fig. 21. PM–AM and PM–PM measured error for calibration and predistortion.

30 GHz with a Marki MM1-1044HS mixer. Two Spacek Labs SG2612-30-24 predrivers are used to amplify 30-GHz RF band signals for large-signal compression measurements, and a Marki FB-3270 bandpass filter is used to filter out the 14-GHz image tone. For modulated signal measurements, the output of the OPA is down-converted back to 8 GHz and demodulated by Keysight Oscilloscope DSAV134A.

One of the significant results in this mm-wave OPA is linearization of the PA with a memoryless lookup table (LUT). This greatly reduces the need for intensive digital signal processing power consumption to implement DPD. While prior outphasing work [34] used a combination of amplitude and phase predistortion to linearize the OPA,

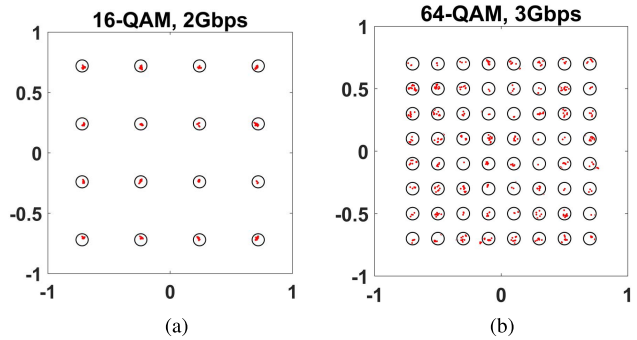

Fig. 22. Constellation plot for different QAMs. (a) Constellation plot for 16-QAM. (b) Constellation plot for 64-QAM.

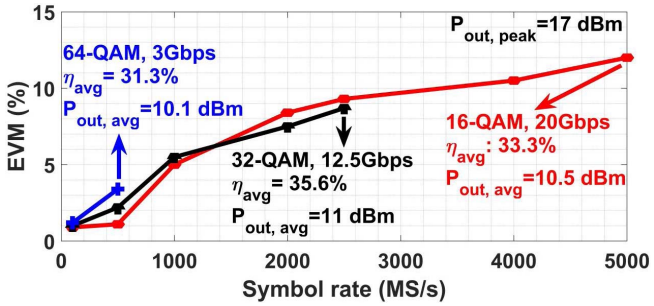

Fig. 23. EVM measurement for different QAM signals at different data rates.

this is an undesirable feature for outphasing, which should be predistorted solely through phase compensation.

As shown in Fig. 20, each QAM symbol is resolved into two outphasing signals where the two signals have common phase ϕ and outphasing phase θ.

Unequal amplitude from two paths of the PA and power combiner causes the actual symbols to have some mismatch with respect to the ideal symbols. In OPAs, the output power is controlled by θ such that both amplitude modulation (AM–AM) is adjusted through the outphasing angle, while the phase modulation (AM–PM) is adjusted through a common-mode phase signal. Therefore, both amplitude and phase calibration are performed solely by phase. Fig. 20 shows that the AM mismatch could be compensated by AM–PM outphasing phase correction $\Delta\theta$ and the PM mismatch could be compensated by PM–PM common phase correction $\Delta\phi$.

The measured AM–AM and AM–PM behavior is shown in Fig. 21. The calibration is normalized to the maximum output power of the outphasing PA to calibrate amplitude and phase, and each deviation is stored in an LUT.

D. QAM Measurements

Fig. 22 plots the 16-QAM and 64-QAM constellations at 500 MS/s. In both cases, the constellation exhibits low EVM. At 100 MS/s, the rms EVM is measured to be under 1.5% for 16-/32-/64-QAM waveforms. Fig. 23 shows a comparison of the EVM for different QAM waveforms at different symbol rates using only the memoryless LUT described previously. In all EVM measurements, the peak power symbol is set to the peak output power (17 dBm) to demonstrate the linearity

TABLE I
COMPARISON OF THIS WORK WITH STATE OF THE ART

	[32]		[21]	[26]		[13]		**This Work**		
Technology	40nm CMOS		130nm SiGe	45nm SOI		130nm SiGe		45nm SOI		
Architecture	Outphasing		Outphasing	Outphasing		Doherty		Outphasing		
Supply (V)	1		4	1		1.5		1.2		
Frequency (GHz)	59.5-67		28	25.5-30		23.3-39.7		30		
Gain (dB)	26		14	-		18.2		7		
P_{sat} (dBm)	15.6		23	17.1		16.8		17		
Peak η (%)	25*		43	56		29.4		50.5		
η @6dB PBO	9*		35	38		25.4		**40**		
Modulation	QPSK	8PSK	64QAM OFDM	64QAM		64QAM		16QAM	32QAM	64QAM
Data Rate (Gb/s)	3.52	-	0.48	6	15	3	6	0.4 2	0.5 2.5	0.6 3
EVM (dB)	-34	-35	-30.5	-29.7	-27.5	-27	-26.6	**-41 -36**	**-38 -28.4**	**-36.4 -28**
P_{avg} (dBm)	10.8	11	14.3	10.7	10.4	9.2	7.2	10.5	11	10.2
η @ P_{avg} (%)	-	-	25.3	36	34	18.5	14.4	**33.3**	**35.6**	**31.2**
Area (mm^2)	0.96		0.56	-		1.76		1.65		
* **for PAE instead of** η										

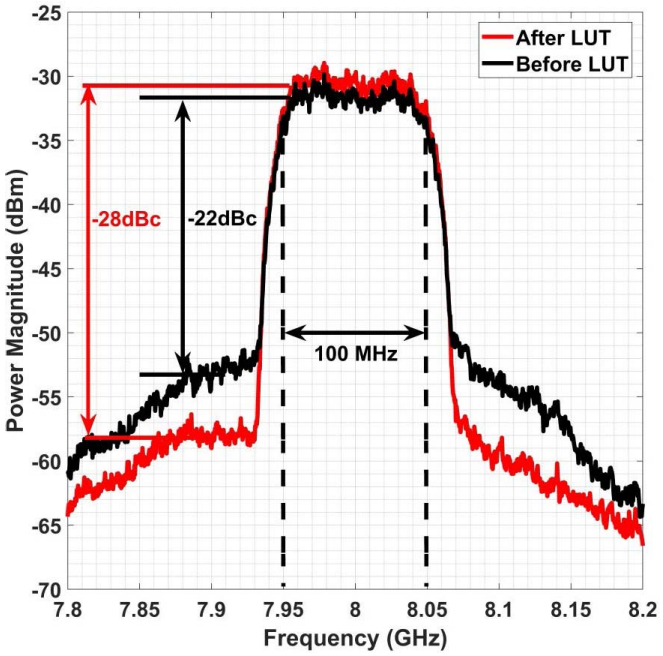

Fig. 24. ACPR of QAM-64 with 100-MHz signal.

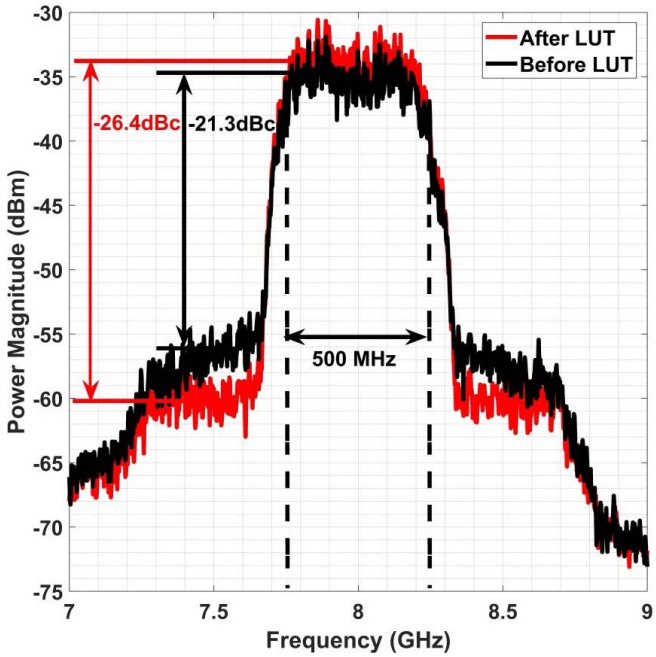

Fig. 25. ACPR of QAM-64 with 500-MHz signal.

under the highest efficiency. The average efficiency η_{avg} for 64-QAM signal at 3-Gb/s data speed is 31.3% with 10.1-dBm average output power. At 16-QAM modulation, the EVM is 12% with a record data speed of 20 Gb/s with 10.5-dBm output power. To the best of our knowledge, this is the first CMOS PA at Ka-band to achieve 20-Gb/s modulated data speed, which is expected by 5G peak data rate.

Figs. 24 and 25 show the ACPR for 64-QAM signal at 100- and 500-MS/s sample rates with and without the phase-only memoryless LUT. The ACPR has 6- and 5-dB improvement after compensation at 100- and 500-MS/s sample speed, respectively, without introducing substantial increased demands in the DAC bandwidth. In this measurement, outphasing angle is controlled by AWG at baseband and the resolution of the outphasing angle directly contributes to the nonlinearity in the outphasing transmitter. In [35] and [36], the DAC resolution directly impacts the ACPR and, in particular, a −40-dB ACLR demands slightly more than 40-dB AM dynamic range. This dynamic range relates to the phase resolution requirement larger than 8 bits.

Table I compares the measured performance of the presented OPA comparing to the state of the art. The presented hybrid-mode OPA achieves the highest OBO efficiency compared to earlier work as well as the lowest EVM and highest peak data rate.

VI. CONCLUSION

This article presents a hybrid-mode OPA that is designed to achieve the highest efficiency in a CMOS process. The hybrid mode realizes a compact, low-loss current-mode power combiner to avoid high losses under backoff power conditions. The CMOS PA design considers the importance of transistor parasitics on load modulation and demonstrates a combination of unilaterization, neutralization, and stabilization to realize a

high-efficiency OPA. The demonstrated OPA achieves a peak η of 50.5% and a 6-dB OBO η of 40% all while operating with true constant envelope input signals. Finally, we demonstrate a memoryless LUT to compensate AM–AM and AM–PM variation of each symbol and demonstrate less than 1.5% EVM at 100-MS/s sample speed. For a 16-QAM signal, the PA achieves highest 20-Gb/s data rate as expected for 5G peak data rate.

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