A Fully Integrated 32 Gbps 2x2 LoS MIMO Wireless Link with UWB Analog Processing for Point-to-Point Backhaul Applications

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***Abstract*— In this paper, we demonstrate a proof-of-concept 130 GHz wireless 2x2 line-of-sight (LoS) multi-input multi-output (MIMO) transceiver using fully packaged transmit and receive arrays and scalable analog baseband processing. The link utilizes the Rayleigh criterion to transmit independent wireless streams over a LoS channel. The transmitter (TX) and receiver (RX) chips are fully packaged with integrated mm-wave antennas. The two-element QPSK TX array consumes 432 mW, while the entire four-channel QPSK MIMO RX consumes 630 mW and supports four concurrent 130 GHz mm-wave channels with a simulated passband bandwidth of 20 GHz. Wireless measurements demonstrate 32 Gbps QPSK transmission over 40 cm, allowing for a link efficiency of 83 pJ/ bit/ m and an energy efficiency of 33 pJ/ bit. Scaling the system from the two channels measured here to the four channels supported by the RX chip will double the data rate as well as the range reported.**

***Keywords*— mm-wave, 5G, eWLB, HDI, SiGe, LoS MIMO, spatial multiplexing, analog processing.**

I. Introduction

Global wireless data traffic has increased exponentially in the past few years and will continue to rise, driven by the demand for mobile multimedia streaming and connectivity. The increasing demand calls for innovative approaches for the design of future systems both in the mobile link and for the backhaul, where the aggregated data from/to multiple users increases super-linearly with the user demand. Mm-wave transmission for user links as well as for backhaul is now commonly accepted due to the high spatial multiplexing degrees of freedom (DoF) as well as larger bandwidth available at mm-wave frequencies. Even in pure line-of-sight (LoS) environments, with reasonable array sizes, multi-stream parallelism can be attained [1]. In a mm-wave LoS multi-input multi-output (MIMO) link, independent streams between localized transmit and receive antenna arrays can be encoded into a set of tightly-spaced beam angles. These streams can be separated using simple analog processing, resulting in throughput multiplication with a reasonable increase in processing complexity [2]. To realize a LoS MIMO link, one approach is to use a general multiple-beamforming (MBF) topology [3]. However, this would result in a sub-optimal implementation with a required total number of beamforming delay lines that scales quadratically with the array size [4]. In LoS MIMO, the synthesized beams between the transmitter (TX) and the receiver (RX) have narrow azimuthal spread. The result is that the true time delay (TTD) settings required for beamforming are quasi-independent from the individual beams, and only vector combining (or spatial equalization) needs to be replicated per stream, considerably reducing the processing complexity. In this work, we present a fully-integrated end-to-end LoS MIMO system utilizing an analog MIMO processor that takes advantage of the special mm-wave LoS MIMO channel properties [2]. Proof-of-concept measurements demonstrates 2×16 Gb/s aggregate throughput in a 2×2 array arrangement. To the authors' knowledge, this paper is the first demonstration of a fully integrated mm-wave LoS MIMO system to date. The paper is organized as follows: Section II describes the architecture of the transceiver system as well as the packaging details. Circuit level details of the proposed RX chip are discussed in section III, while the details of the standard single-element TX chip are outside the scope of this paper. Section IV discusses the measurement results and Section V concludes the paper.

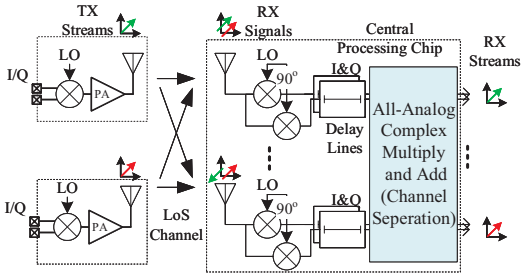


Fig. 1. Block diagram of a 2×2 LoS MIMO system, with the TX and RX signals shown as vectors in the I/Q domain

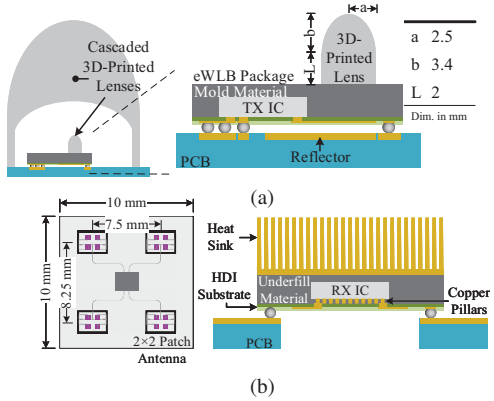


Fig. 2. Assembly diagram of (a) the TX package, and (b) the RX package

II. Transceiver Architecture, Integration, and Packaging

Fig. 1 shows our proposed fully-integrated LoS MIMO system. The proposed system utilizes the spatial DoF in

all three dimensions to maximize range and capacity: the depth (vertical dimension) in the TX lens to improve the TX directivity, and the spread (lateral dimension) in the RX package to enable the spatial multiplexing. The system, shown in Fig. 1 shows a 2×2 LoS MIMO link. The transmit array consists of two embedded wafer-level BGA (eWLB) packaged QPSK TX elements. Each eWLB package carries a complete 130 GHz mm-wave TX, with an in-package antenna as well as 3D printed lenses for improved directivity and gain. On the RX side, a high density interconnect (HDI) BGA package carries the four-channel mm-wave MIMO RX chip, as well as four sets of 2×2 aperture-feed patch antenna arrays similar to the work in [5]. The received signal from each antenna array is routed on the package to a single four-channel MIMO RX chip. In this paper, we only provide the measurement results for two of the four channels supported by the proposed RX chip.

A. Transmitter Package

The transmit array consists of two identical TX elements, synchronized to the same 16.25 GHz external LO, each transmitting an independent QPSK stream. The TX chip contains two independent pseudo-random bits sequence (PRBS) generators integrated on-chip for testing, a three-stage active push-push frequency multiplier to generate quadrature 130 GHz LO signal from the external 16.25 GHz LO, a quadrature Gilbert mixer followed by a two-stage standard differential cascode PA. The PA drives an antenna on the eWLB package that illuminates a low-cost 3D-printed Lens to achieve a peak EIRP of 28 dBm. The QPSK TX chip circuit details are outside the scope of this paper. Fig. 2(a) shows the assembly diagram of the TX element used in his work. The eWLB package is based on an embedded device technology with a high-resolution fan-out redistribution layer (RDL) [6]. While eWLB can support multiple thin-film RDL layers, this design uses one RDL layer to reduce the fabrication cost. Coplanar waveguide (CPW) techniques were adopted in this design to enable the use of a single RDL layer for the mm-wave structures. The mold layer in the eWLB package was thinned down to 250 μm, to allow for better radiation performance without sacrificing the mechanical strength of the package. The simulated effective dielectric constant of the eWLB mold is estimated to be 2.6.

B. TX Integrated Lenses

To keep the alignment process of the transmit array within reasonable complexity, the target directivity of the TX element is kept at 30 dBi. To achieve this directivity level, we adopted a stacked lens structure using two sets of 3D-printed lenses as shown in Fig. 2(a). The larger lens (the outer lens) is a dome-type elliptic lens with a 40 mm base diameter and 45 mm height, similar to the lens described in [5]. For this lens, an illumination directivity of around 11 dBi is necessary for proper operation. To achieve this directivity, we use a smaller lens attached to the backside of eWLB package, which provides two functions:

- Impedance matching and BW enhancement: using a step layer between the mold of the eWLB package and air, providing a transition in the permittivity between the two mediums.
- Directivity: the small lens helps focus the beam from the patch antenna on the eWLB package and reduces the sidelobes and the surface modes.

The design parameters of the small lens are shown in Fig. 2 (a), which are derived using the technique described in [7] and later refined using EM simulations. Both lenses are 3D printed using low-cost ABS-M30 material (used extensively in classic 3D printers), with a measured dielectric constant $\epsilon_r = 2.48 - j0.027$ at 140 GHz.

C. Receiver Package

The main design goal of the RX package is the integration of a 2×2 MIMO antenna array with an energy-efficient mm-wave RX chip. To achieve this goal the packaging solution for the RX chip needs to meet the following criteria: (1) an adequate separation between the elements to enable a longer communication range, (2) good isolation between the antenna elements, and (3) highly accurate patterning for proper mm-wave impedance control. Fig. 2 (b) shows the integration scheme that is employed for the RX package. The RX chip is assembled on the BGA using flip-chip bonding and copper pillar technology (pad ring pitch of 100 μm). The integration of the antennas and the silicon on the same package confines all mm-wave signal routing on the package itself, while only DC and low-frequency signals are routed to the main PCB board through standard 300 μm solder balls. The chip-on-top assembly is shown in Fig. 2 (b), with the mm-wave radiation through an opening in the PCB board, allows for heat dissipation from the high-performance chip from the backside, using a suitable heat sink attachment.

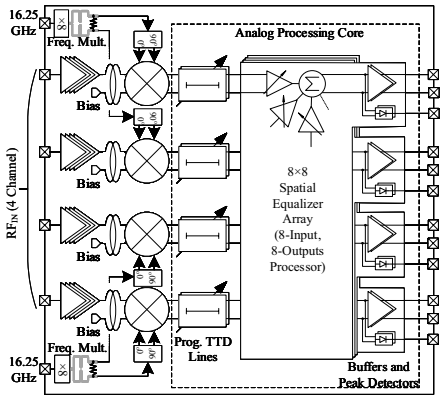


Fig. 3. Block diagram of the RX chip showing the main building blocks.

III. Receiver Circuits and Building Blocks

On the RX package, shown in Fig. 2(b), the 130 GHz MIMO data is captured at each one of the four antenna arrays and then routed through microstrip transmission lines to the central RX Chip. Fig. 3 shows the RX chip block diagram. The chip supports four simultaneous QPSK channels and includes the necessary RF front-ends and analog baseband processing required for MIMO reception and channel separation.

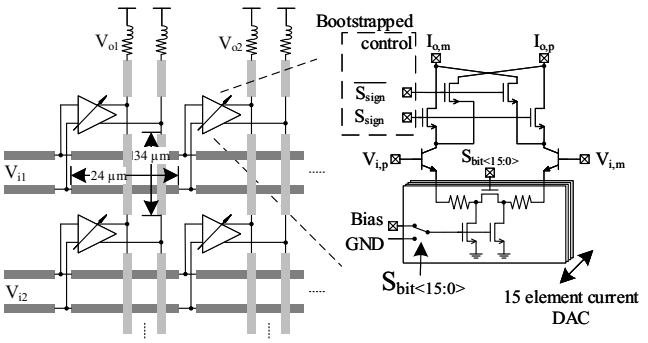


Fig. 4. CSN spatial equalizer.

A. Mm-wave Front-ends

The mm-wave signal is first fed into a 4-stage 130 GHz LNA, with the bias current for each stage optimized independently for optimum noise figure (NF) and gain. The simulated gain and NF of the LNA are 30 dB and 9.5 to 10 dB, respectively. The current of the LNA stages 2 to 4 is programmable per channel, to correct for the individual channel gains and PVT variations. The received signal is then fed into a quadrature Gilbert mixer for direct downconversion. The LO signal for the mixer is generated using a pair of three-stage active push-push frequency multipliers (one for every two channels), a set of two Wilkinson power dividers, and four quadrature hybrids and 130 GHz LO buffers. The output of the mixer is then filtered and fed into the baseband processor for MIMO processing.

B. LoS MIMO Analog Processor Design

The two main processing functions of the analog processing core are: (1) an array of true-time delay (TTD) elements and (2) an analog spatial equalizer. For this proof-of-concept demonstration with a relatively small aperture at the RX array, only broadside measurements are conducted and hence no TTD delay correction was needed.

After the TTD stage, signals are fed to an 8×8 analog spatial equalizer, consisting of 64 programmable-gain amplifiers (PGAs) with current mode summation for signal reconstruction (Fig. 4). Each PGA implements multiplication of the UWB signal with a static 5-bits signed coefficient. The sign bit of the coefficient modulates the output current of the PGA using high-speed thin-oxide bootstrapped NMOS switches for low voltage operation without sacrificing the speed, while the remaining 4-bits control the PGA input stage bias current with 40-μA resolution. To minimize the accumulation of path-dependent parasitic delay while traveling through the spatial equalizer lines, the layout of the PGA cell is optimized to fit into a small area of $24\,\mu\mathrm{m} \times 34\,\mu\mathrm{m}$. After spatial equalization, the resulting outputs are buffered by CML drivers that drive off-chip 100-Ω differential loads. The envelopes of the output signals are monitored using on-chip low-power low-offset peak-detectors. Such envelope information can be used for channel identification using the technique described in [2].

IV. MEASUREMENT RESULTS

The TX and RX chip are fabricated in 55 nm SiGe technology and packaged using eWLB and HDI technologies, respectively. Fig. 5 shows the die photo of the RX chip as well as the packages micrographs. Fig. 6(a) shows the frequency-domain test setup for the TX chip used to measure the radiation pattern of the TX antenna and lens structure. The transmission BW is believed to be limited by the on-chip antenna matching, which is shown in Fig. 6(b). Fig. 6(c) shows the normalized measured radiation pattern of the complete TX package using the small lens as well as the two lens stack.

Fig. 7(a) shows the test setup for the wireless link of the 2×2 MIMO system. In this measurement, the TX array and the RX module are placed in a line-of-sight configuration with a 40 cm spacing. The TX and the RX element separation is 6 cm and 7.5 mm, respectively, which satisfies the separation for Rayleigh spacing in LoS MIMO for a 40 cm link [1]. The two TX chips and the RX chip are synchronized using the same 16.25 GHz LO signal from a Keysight 8311B signal generator. The TX QPSK data are generated using the on-chip PRBS generators (each supplying an independent PRBS-7 sequence, with one of the TX inputs connected to the Keysight N4903B generator for bit error rate testing (BERT)). Channel estimation is done with the aid of a computer-run algorithm and the R&S FSW43 spectrum analyzer. The correct coefficient for the channel is then loaded through SPI connection to the RX memory, and the resulting output baseband signal is fed into the bit detector of Keysight N4903B, where clock and data recovery operations are performed. The performance of the channel separation is demonstrated in Fig. 7(b), which shows the frequency spectrum of two received channels, running at 8 Gbps each, with and without the channel separation, showing around 10 dB of isolation across the band of interest. The link is measured to have a bit error rate (BER) of 10^{-3} at 40 cm. Fig. 7(c) and (d) show the measured received eye diagram at 20 Gbps (5 Gbps×2 active complex channels) and 32 Gbps (8 Gbps×2 active complex channels), respectively. The simulated BW of the RX chip is over 20 GHz at 130 GHz, and the data rate limitation in this measurement is believed to be due to the matching BW of the patch antenna at the TX module. Table 1 compares this work to state-of-the-art wireless transceivers.

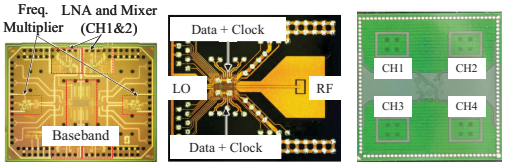
V. CONCLUSION

A fully packaged LoS MIMO transceiver system is presented in this paper. The TX and RX chips are fabricated in 55 nm SiGe (f_T/ f_{max} of 320 GHz/ 370 GHz) technology and achieve a data rate of 32 Gbps over 40 cm range. The chip utilizes baseband analog processing techniques to enable compact, broadband and low-power MIMO processing of the received streams. The TX and RX chips are fully packaged, with embedded mm-wave structures on the packages. Only two of the four channels supported by the RX chip were used, suggesting the capability of doubling the range and data rate reported in this paper. To the authors' knowledge, this paper is the first demonstration of a fully integrated mm-wave LoS MIMO system to date.

Table 1. Performance Summary and Comparison

Ref.	[8]	[9]	[10]	This Work
Tech.	65nm CMOS	55nm BiCMOS	28nm CMOS	55nm BiCMOS
f_c [GHz]	70-105	130	60	130
Data Rate [Gbps]	120	12.5	27.8	32 (64*)
Modulation	16QAM	OOK	16QAM	QPSK
DC Power [mW]	TX:120 RX:160	TX:59 RX:38	TX:210 RX:110	TX:432 RX:630
Range [m]	0.2	5	0.05	0.4 (0.8*)
Energy Efficiency [pJ/bit]	2.3	7.76	11.5	33
TX P_{out}/ element [dBm]	-1.9	9.5 (Nom.)	4	2.5
FoM [pJ/bit/m]	11.6	1.55	230	83
Integration Level	Chip+Ext. Horn	Fully Packaged	Fully Packaged	Fully Packaged
MIMO Streams	1	1	2	2 (4*)
Die Area [mm^2]	6	3.2	3.9	8

*Estimated range and data rate improvements when using the full four channels of the RX chip.



(a) (b) (c)

Fig. 5. Die photos of Rx chip, as well as the micrograph of (b) TX package and (d) RX package.

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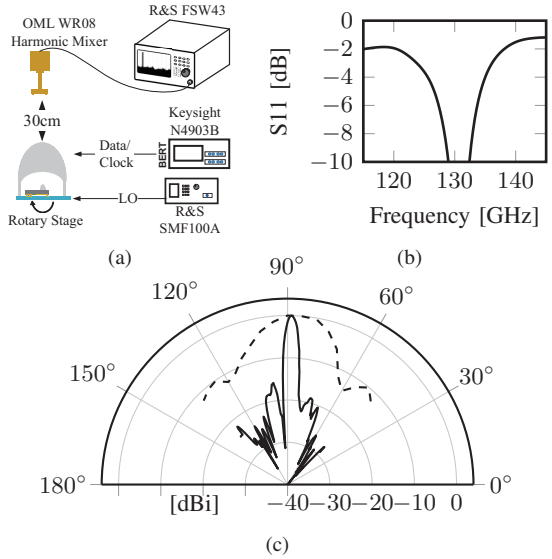
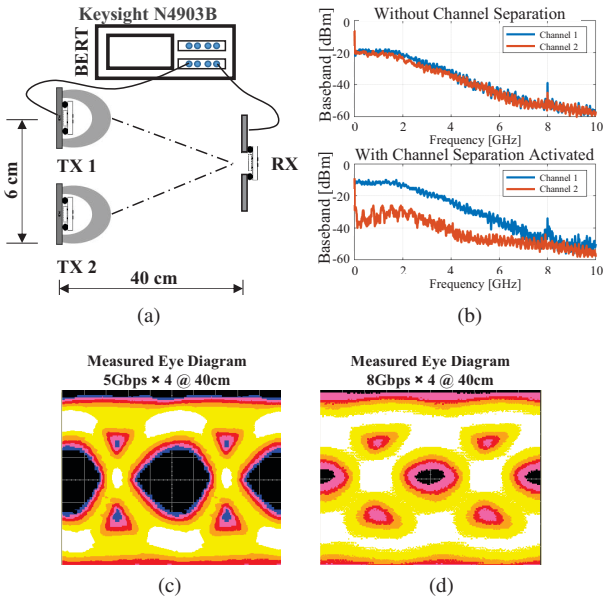


(a) (b) (c)

Fig. 6. (a) Frequency domain test setup for the eWLB TX. (b) Simulated input matching of the on-package coplanar antenna and (c) measured radiation pattern of the small lens (dashed) and the two lens stack (solid)



(a) (b) (c) (d)

Fig. 7. (a) test setup for 2×2 wireless MIMO Transmission, (b) measured frequency domain channel separation, (c) Measured eye diagram at 5 Gbps per real dimension and (d) at 8 Gbps per real dimension.

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