A Fully Packaged 130-GHz QPSK Transmitter With an Integrated PRBS Generator

Mahmoud Sawaby, Nemat Dolatsha, Baptiste Grave, Cheng Chen, and Amin Arbabian

***Abstract*—This letter presents a fully packaged 130-GHz QPSK transmitter (TX) with an on-package Vivaldi antenna for high-density dielectric waveguide (DWG) chip-to-chip and board-to-board interconnects. The TX chip contains a multiplier chain for the local oscillator path, up-conversion mixers, and a two-stage power amplifier. For testing, the chip also includes two $2^7 - 1$ sequence-programmable high-speed pseudo-random bit generators, each capable of generating 18 Gb/s (limited by test equipment) at energy efficiency of 0.7 pJ/bit. The fully packaged TX achieves a data rate of 36 Gb/s over a 1-m-long DWG link, leading to energy efficiency of 6 pJ/bit.**

***Index Terms*—Dielectric waveguide (DWG), high-speed links, mm-wave circuits, pseudo-random bit sequence (PRBS), SiGe, transmitter (TX), Vivaldi antenna.**

I. Introduction

The demand for higher communication bandwidths in data centers and for backhaul transmission is fueled by new 5G and IoT applications and is growing at a fast rate. At the same time, the traditional trends of high-rate communication links have benefited from the steady increase in transistor transit frequencies (f_T) and maximum oscillation frequencies (f_{max}), allowing for faster baseband processing, as well as higher center frequencies of operation for transmission. With the 60-GHz implementations already transitioning to products, the focus of current designs is to utilize higher frequencies, for example, the 130-GHz band and above, where the capacity improves by access to more bandwidth as well as larger spatial degrees of freedom [1].

High-speed and short to medium reach copper interconnects have been extensively studied in literature as the primary communication mechanism for chip-to-chip and board-to-board links. An alternative communication medium, currently enabled by advances in mm-wave technology and packaging, is low-loss dielectric waveguide (DWG) links [2]. These waveguides present lower loss and dispersion, and the challenge turns into designing efficient and dense interfaces from the chip to the guided modes of the link. In this letter, we present a fully packaged 130-GHz transmitter (TX) silicon chip with an integrated Vivaldi-like structure optimized to gradually couple into the DWG for wide-band mm-wave transmission. The TX chip uses an external 1/8 local oscillator (LO) signal to up-convert and modulate QPSK data to a carrier frequency of 130 GHz. The chip also includes two pseudo-random bit sequence (PRBS) generators that can be used for testing purposes by supplying random I/Q data sequences for the QPSK modulator. The modulated output feeds into a ground-signal-ground interface into an on-package wideband Vivaldi antenna. The following sections describe the details of the system architecture and measurement.

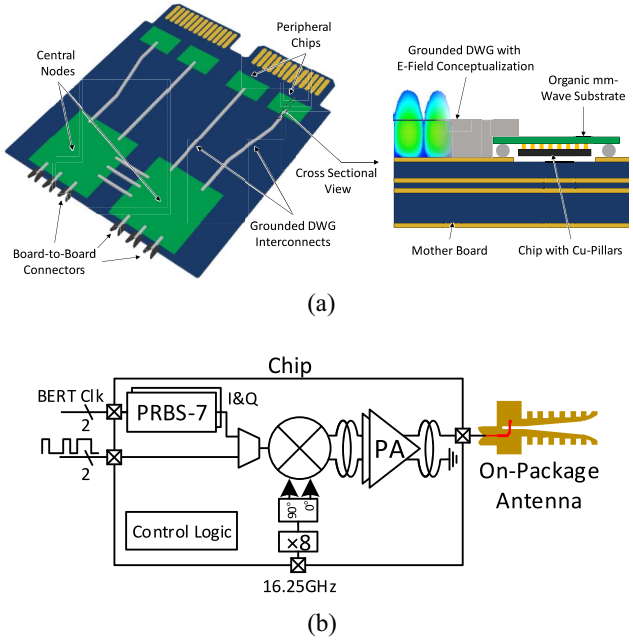

Fig. 1. (a) Cross section of the proposed TX element package. (b) Block diagram of the TX chip.

II. Architecture Overview

The proposed chip-to-chip and board-to-board interconnection networks using low-loss DWG is conceptualized in Fig. 1(a). Fig. 1(b) shows the block diagram of the TX chip. Detailed discussion of different blocks is provided below.

A. Programmable Pseudo-Random Bit Generator

For testing purposes, two high-speed current-mode-logic-based programmable PRBS generators were designed and integrated into the proposed TX chip. The main features of the proposed PRBS generators are: 1) sequence-programmability, allowing the same circuit to generate eight different codes, enabling potential scaling into higher order modulations and 2) full-rate operation, such that each PRBS generator can feed the modulator with full-speed testing streams. The following techniques were adopted to maximize the speed of the PRBS generator.

1) Although the target PRBS length was 7 bits, the design implemented a longer (9 bits) flip-flop chain. The longer chain enables the flexibility of having fewer taps on the feedback

Manuscript received October 23, 2018; revised December 27, 2018; accepted January 19, 2019. Date of publication January 25, 2019; date of current version February 11, 2019. This paper was approved by Associate Editor Andrea Mazzanti. This work was supported in part by ComSenTer, one of six centers in JUMP, a Semiconductor Research Corporation program sponsored by the Defense Advanced Research Projects Agency, in part by Texas Instruments, and in part by the National Science Foundation under Grant CNS-1518632. *(Corresponding author: Mahmoud Sawaby.)*

M. Sawaby, N. Dolatsha, C. Chen, and A. Arbabian are with the Department of Electrical Engineering, Stanford University, Stanford, CA 94305 USA (e-mail: msawaby@stanford.edu).

B. Grave is with the Department of Electrical Engineering, Stanford University, Stanford, CA 94305 USA, and also with CEA, LETI, 38054 Grenoble, France.

Digital Object Identifier 10.1109/LSSC.2019.2895571

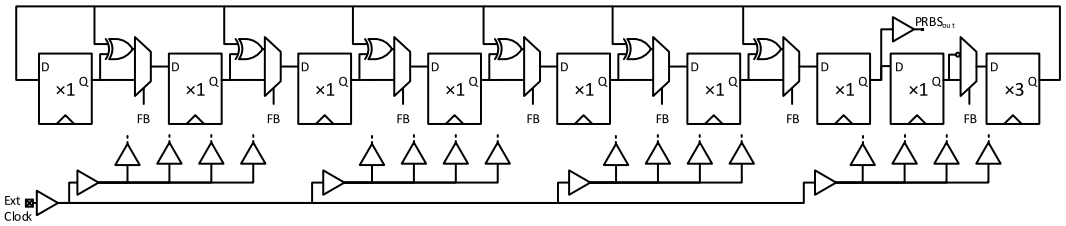

Fig. 2. Block diagram of the PRBS-7 block.

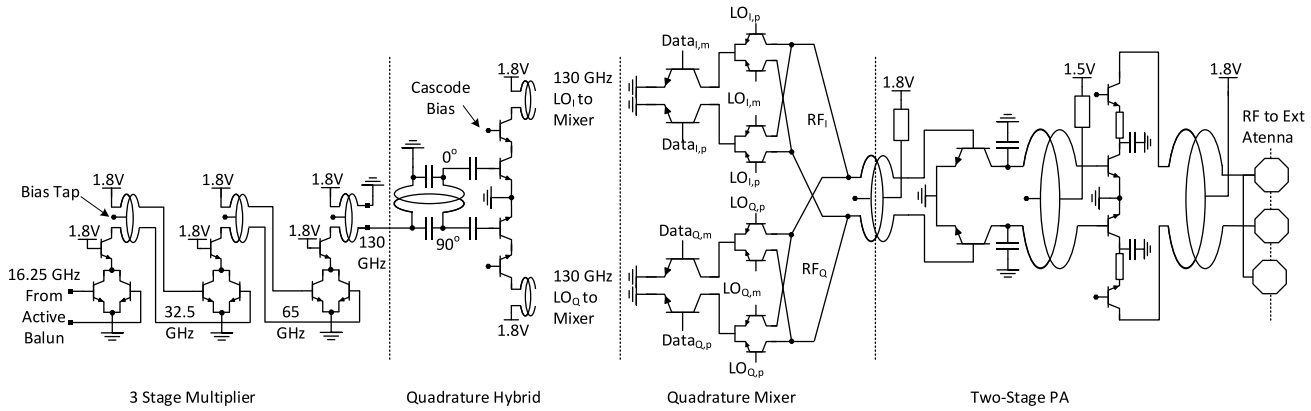

Fig. 3. Schematic of the TX chain showing: (left to right) (a) frequency multiplier, (b) quadrature hybrid, (c) quadrature mixer, and (d) two-stage PA.

path of the PRBS generator loop, as shown in Fig. 2, relaxing the loading on the critical feedback path. Different lengths (7, 8, 9, and higher) were examined for this design, and a chain of 9 flip-flops was found to require the least number of feedback taps while enabling the programmability of the generator.

2) The two-stage XOR-MUX logic used for programming the feedback of the PRBS generator loop is optimized to minimize the delay through the feedback arc of this complex gate. This relaxes the timing constraint on the feedback path and improves performance.
3) The drive strength of the last stage of the PRBS generator loop is optimized ($\times 3$) such that no additional buffer is required in the feedback path, reducing the power consumption without sacrificing the speed.

The measured bit rate for each PRBS generator was 18 Gb/s at a power consumption of 90 mW each, resulting in an energy efficiency of 0.7 pJ/bit. Table I compares the proposed PRBS generator with current state-of-the-art, and shows that this design provides a competitive energy efficiency per bit compared to current literature. The details of the measurement setup are presented in Section IV.

TABLE I
COMPARISON WITH HIGH-SPEED PRBS GENERATORS ON SILICON

Ref.	Tech.	Power [mW]	Rate [Gbps]	Length	FoM [pJ / bit]
[3]	SiGe	243	23	2^7-1	1.51
[4]	SiGe	1000	80	$2^{11}-1$	1.14
[5]	SiGe	1700	80	$2^{15}-1$	1.42
This Work	SiGe	90	18	2^7-1	0.7

$$\text{FoM} = \frac{\text{Power Consumption}}{\text{Data Rate} \times \log_2(\text{PRBS Length})}$$

B. TX Chain

The chip contains all the required LO generation and modulation circuitry required for QPSK transmission at 130 GHz. The TX chain main components are described below.

1) LO Generation: The LO chain converts the single-ended 16.25-GHz external LO into 130-GHz quadrature signals. The core of this chain is the frequency multiplier composed of three cascaded differential frequency doublers, as shown in Fig. 3. To minimize the area of the first stage, an active balun (instead of a bulky transformer-based balun) is used to generate the differential input of the first doubler from the single-ended external LO input. I/Q generation is performed by the transformer-based hybrid shown in Fig. 3 [6]. The output of the hybrid is then buffered and fed to the quadrature mixer.

2) Quadrature Mixer: A Gilbert-based quadrature mixer is used to up-convert data bits onto a QPSK-modulated 130-GHz carrier frequency. QPSK modulation was chosen for the simplicity of its implementation without sacrificing the spectral efficiency. A schematic of the mixer is shown in Fig. 3. The mixer consumes 10 mA from a 1.8-V supply, with a single sideband BW of 15 GHz. The center-tap of the secondary side of the output transformer of the mixer includes a parallel resonant network to suppress common-mode signals and ensure stability while feeding into the power amplifier (PA) [7].

3) Power Amplifier: The PA schematic is shown in Fig. 3, which consists of a two stage common-source and cascode differential amplifiers. The first stage uses a supply voltage of 1.5 V, and is used to provide additional gain to the PA chain. The second power stage is a cascode to allow for slightly higher supply voltage (1.8 V) and improved stability. To enhance the maximum available gain (MAG) of the second stage, interstage matching inductors are used in between the common-source and the cascode stages [8], improving the simulated MAG by 1.5 dB. The low-loss nature of the DWG channel requires a relatively low transmit power even for moderate lengths of the link (meters). The designed PA provides an output power of 2.5 dBm from 1.8-V supply.

TABLE II
COMPARISON WITH STATE-OF-THE-ART DWG TXS

Ref.	Tech.	fc / BW [GHz]	Rate [Gbps] / Mod.	P_{out} [dBm]	pJ / bit	pJ / bit / P_{out}	DWG Dimensions [mm]	DWG Length [m]	Pitch* [mm]	Rate / Pitch [Gbps/cm]	Package Loss [dB]	Integration Level
[12]	40 nm CMOS	120 / 10**	12.7 / CP-FSK	-	-	-	2 (Circular)	1	4	31	-	Fully Packaged with Vertical DWG Coupling
[10]	40 nm CMOS	120 / 10**	18 / CP-FSK	-1.9	0.7	1.1	2 (Circular)	1	4	45	3.4	Fully Packaged with Board-Edge DWG Coupling
[13]	65 nm CMOS	300 / 40	30 / QPSK	-6	6	23.8	No DWG Measurements					Fully Packaged
This Work	55 nm SiGe HBT	130 / 40	36/ QPSK	2.5	6	3.5	1.3 ×1.3	1	2.6	138	3	Fully Packaged with On-Board and Board-Edge Coupling Capability

* Based on simulation for > 25 dB isolation between adjacent lines, ** Estimated

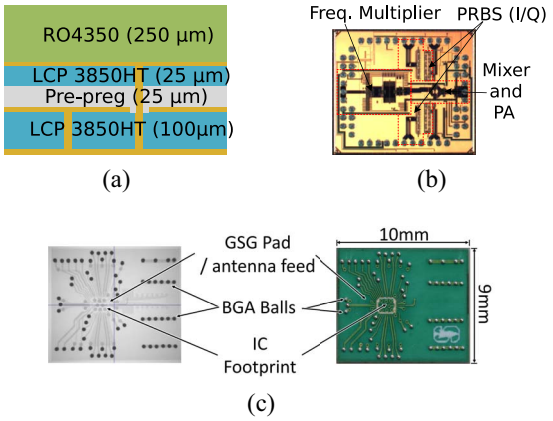

Fig. 4. (a) Layer stack for the custom organic substrate. (b) Chip micrograph. (c) Interposer substrate X-ray image and photograph.

III. PACKAGING AND DWG FEED DESIGN

Different feed structures have been proposed in literature in order to synthesize the correct mode to feed the DWG [9]–[11], with some requiring the DWG to be inserted on top of an antenna array for improved coupling efficiency. In this letter, we focus on low-profile and efficient planar coupling solutions that allow for on-board high-speed communications as well as board edge interfaces in high-density rack configurations. In the proposed solution, we adopt an intermediate substrate interface (interposer) that incorporates all the mm-wave routing and coupling structures [Fig. 1(a)]. The interposer substrate is based on the high-frequency-compatible Rogers 4350 material, with the stack shown in Fig. 4(a). The substrate carries a flip-chip bonded silicon IC using copper pillar technology, providing a robust and well-defined interface for the mm-wave signals. The substrate itself is later flip-chip bonded to a low-cost FR4 motherboard for signal and data routing, reducing the cost of the system.

The feed structure is based on a Vivaldi antenna design that is optimized to synthesize the required horizontal electric field to generate the TE_X^{11} fundamental mode on the 1.3 mm × 1.3 mm DWG used. As the first characterization step, the free-space radiation pattern of the feed structure is measured to verify the design in comparison to the simulated results in Fig. 5. Measurements show a small coupling loss of 3 dB, stemming from packaging and mode loss from the chip to the DWG, when compared to the direct probing of the silicon die.

IV. MEASUREMENTS SETUP AND RESULTS

Fig. 6 shows the detailed block diagram for the measurement setup for the frequency- and time-domain results. The chip is fed with a

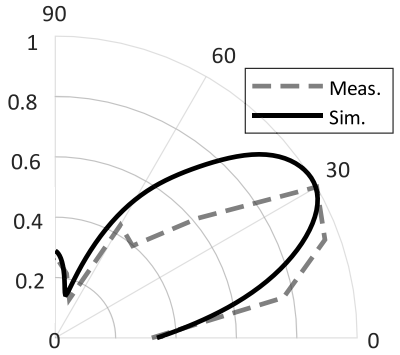

Fig. 5. Simulated and measured free-space radiation pattern of the designed Vivaldi coupler. Simulated beam assumes a corrected dielectric constant of 2 for the Rogers substrate at 130 GHz.

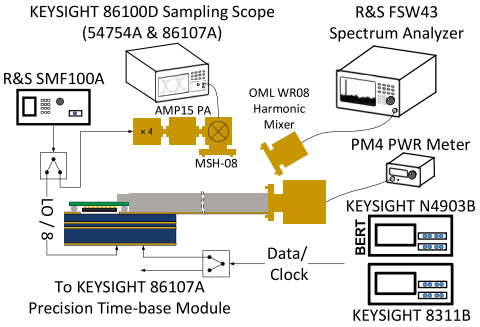

Fig. 6. Measurement setup block diagram.

−6 dBm 16.25-GHz LO signal. For symbol rates up to 12.5 GSps, a KEYSIGHT N4903B bit-error-rate tester (BERT) module is used to feed the chip with the required I and Q data. Above 12.5 GSps, the integrated PRBS generators are activated and the data clock is supplied from a KEYSIGHT 8311B signal source. A 1-m-long DWG is used as the test channel for time-domain measurements. The output power of the package is measured using a calibrated VDI-Erickson PM4 power meter and is measured to be at −0.5 dBm, indicating 3-dB total loss through the package compared to the direct probing of the TX die.

Time domain results are obtained using a second harmonic Millitech MSH-08 down-conversion mixer, which is phase-locked to the LO signal fed to the chip, with the IF output fed to a KEYSIGHT 86100D sampling scope frame. The measured eye diagram plots at 25 Gb/s, 30 Gb/s, and 36 Gb/s are shown in Fig. 7. Bit-error-rate data is also provided at 25 Gb/s and not the higher speeds due to

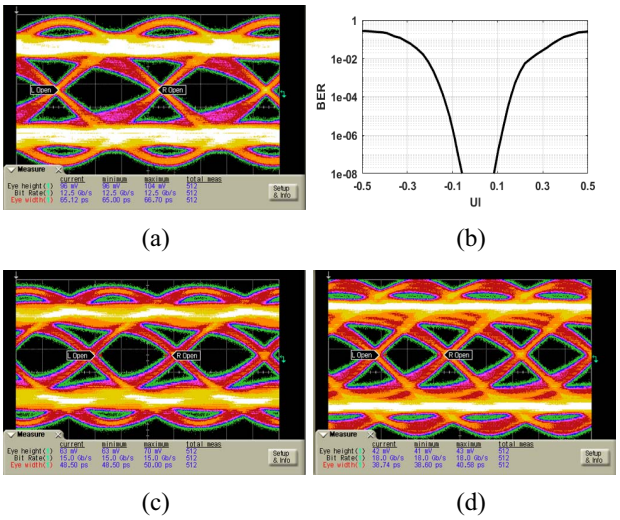

Fig. 7. (a) Measured eye diagram and (b) bathtub curve at 25 Gb/s, as well as at (c) 30 Gb/s and (d) 36 Gb/s (only in-phase component of data is shown).

limitations of the equipment used (KEYSIGHT N4903B BERT module). The chip consumes 220-mW of power at an output power of 2.5 dBm. Table II summarizes the performance of this letter compared to current state-of-the-art. To our knowledge, this letter presents the highest data rate silicon-based transmission over DWG channels to date.

V. Conclusion

A fully packaged 130-GHz QPSK TX is presented in this letter. The TX chip is fabricated in a 55-nm SiGe (f_T/f_{max} of 320 GHz/370 GHz) technology and achieves a transmitted bit rate of 36 Gb/s over a 1-m DWG channel. For testing purposes, the chip also includes two sequence-programmable PRBS-7 generators that operate at 18 Gb/s each, resulting in an energy efficiency of 0.7 pJ/bit. The chip is packaged on a low-cost organic substrate with an antenna on the package for low-loss coupling of the RF signal.

Acknowledgment

The authors would like to thank STMicroelectronics for the foundry donation, NAMICS Tech., Integrand Software for their EMX software, and the Nano@Stanford labs and Stanford Nano Shared Facilities (SNF and SNSF), under NSF award number ECCS-1542152.

References

[1] M. Sawaby, B. Mamandipoor, U. Madhow, and A. Arbabian, "Analog processing to enable scalable high-throughput mm-wave wireless fiber systems," in *Proc. 50th Asilomar Conf. Signals Syst. Comput.*, 2016, pp. 1658–1662.

[2] P. Reynaert *et al.*, "Polymer microwave fibers: A blend of RF, copper and optical communication," in *Proc. 42nd Eur. Solid-State Circuits Conf. (ESSCIRC)*, 2016, pp. 15–20.

[3] E. Laskin and S. P. Voinigescu, "A 60 mW per lane, 4× 23-Gb/s $2^7 - 1$ PRBS generator," *IEEE J. Solid-State Circuits*, vol. 41, no. 10, pp. 2198–2208, Oct. 2006.

[4] A. Gharib, R. Weigel, and D. Kissinger, "A versatile 10–80-Gb/s PRBS-based broadband transmitter with arbitrary 20–60-GHz spectrum shifting," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 11, pp. 3654–3666, Nov. 2016.

[5] M. Khafaji, G. Belfiore, R. Henker, and F. Ellinger, "A 2×2 80 Gbps $2^{15} - 1$ PRBS generator with three operational modes and a clock divider," in *Proc. IEEE Int. Microw. Symp. (IMS)*, 2017, pp. 141–144.

[6] M. Tabesh, A. Arbabian, and A. Niknejad, "60GHz low-loss compact phase shifters using a transformer-based hybrid in 65nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, 2011, pp. 1–4.

[7] N. Deferm and P. Reynaert, "Differential and common mode stability analysis of differential mm-wave CMOS amplifiers with capacitive neutralization," *Analog Integr. Circuits Signal Process.*, vol. 80, no. 1, pp. 1–12, 2014.

[8] W.-S. Kim, X. Li, and M. Ismail, "A 2.4 GHz CMOS low noise amplifier using an inter-stage matching inductor," in *Proc. 42nd IEEE Midwest Symp. Circuits Syst.*, vol. 2, 1999, pp. 1040–1043.

[9] Y. Kim, L. Nan, J. Cong, and M.-C. F. Chang, "High-speed mm-wave data-link based on hollow plastic cable and CMOS transceiver," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, no. 12, pp. 674–676, Dec. 2013.

[10] N. Van Thienen, Y. Zhang, M. De Wit, and P. Reynaert, "An 18Gbps polymer microwave fiber (PMF) communication link in 40nm CMOS," in *Proc. 42nd Eur. Solid-State Circuits Conf. (ESSCIRC)*, 2016, pp. 483–486.

[11] N. Dolatsha, N. Saiz, and A. Arbabian, "Fully packaged millimetre-wave dielectric waveguide with multimodal excitation," *Electron. Lett.*, vol. 51, no. 17, pp. 1339–1341, Aug. 2015.

[12] W. Volkaerts, N. Van Thienen, and P. Reynaert, "10.2 An FSK plastic waveguide communication link in 40nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2015, pp. 178–179.

[13] Q. Zhong *et al.*, "300-GHz CMOS QPSK transmitter for 30-Gbps dielectric waveguide communication," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, 2018, pp. 1–4.