RINGS
Resilient and Intelligent NextG Systems

Massive Extended-Array Transceivers for Robust Scaling of All-Digital mmWave MIMO

Project Number 2148303

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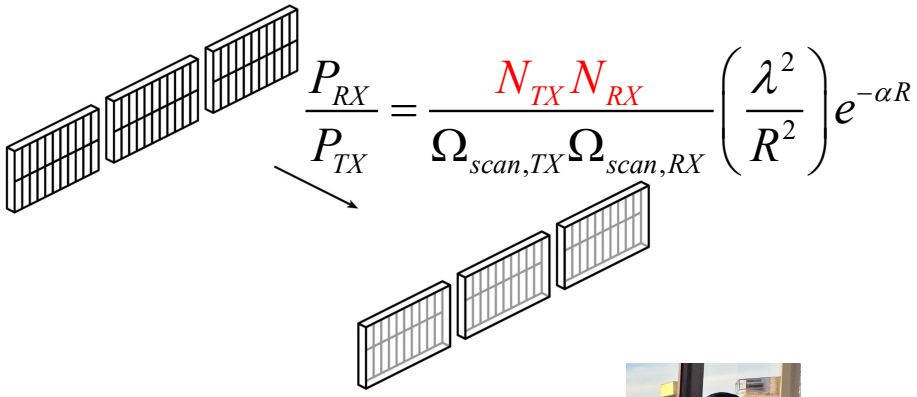
Objective(s)

- Hardware/signal processing co-design for radical scaling
- All-digital mmWave MIMO
  - Spatial scaling: tiled architecture
  - Bandwidth scaling: reduce required dynamic range
  - Computational scaling: exploit channel sparsity
- Radically simplified beamforming
  - Switch-based phase control for large power efficiency gains
  - Innovative tiled architectures alleviating packaging difficulties
  - RF and hybrid beamforming



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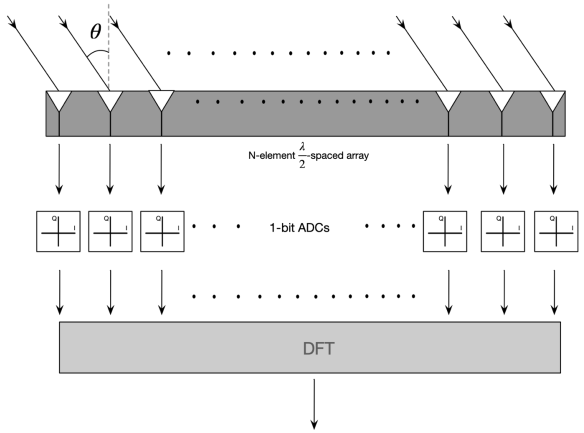
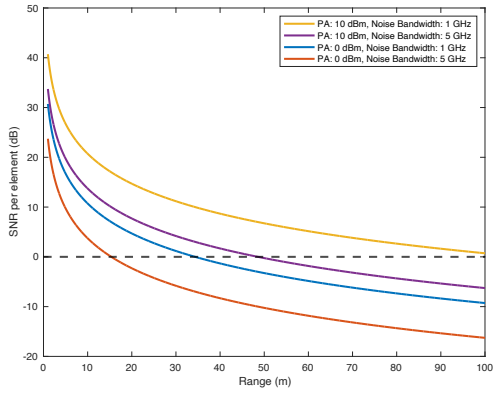
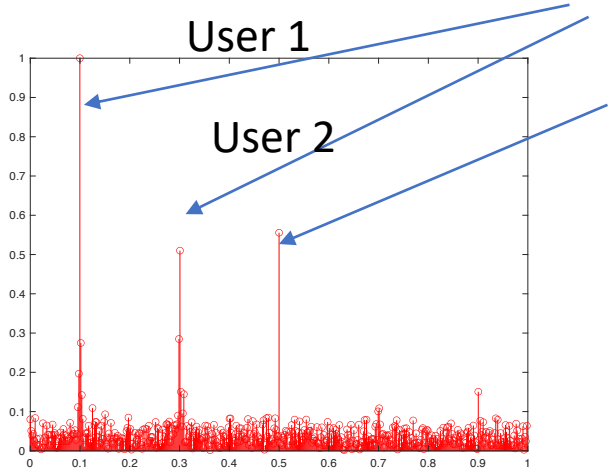
Key Accomplishments (1)

- What might go wrong with low precision?
  - SNR too high (!), channel too sparse, not enough users ➔ input to ADC not Gaussian, noise does not provide dithering
  - Novel Fourier analysis of mmWave MIMO with 1-bit ADC ➔ prescriptions for design and choice of operating regime





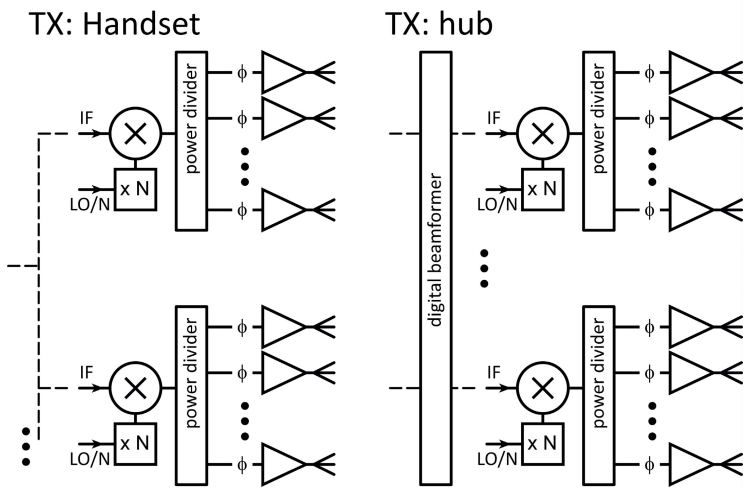
Fundamental frequencies



Harmonic mixture

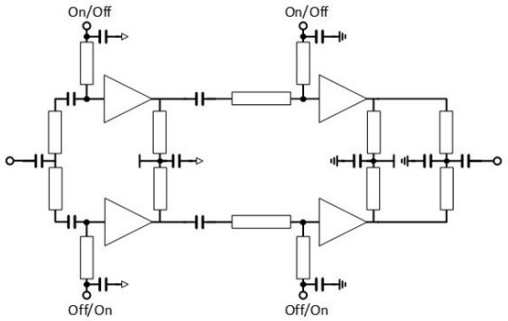
Key Accomplishments (2)

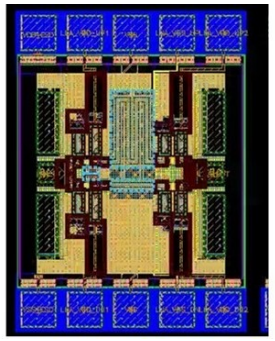
- How to alleviate packaging difficulties while scaling?
  - RF beamformers with switched phase control ➔ compact electronics
  - Tiling to create large arrays ➔ enable RF or hybrid beamforming
  - CMOS electronics + dielectric lenses

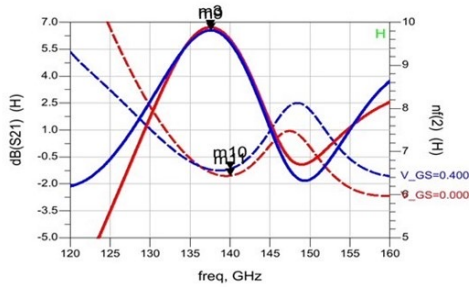


Challenges

- Semiconductor process for initial hardware design was discontinued!
  - Promising test structures in GF 45RFSOI: 6.5 dB gain, 6.5 dB noise figure, 10 mW DC power per element
  - Now upgrading and transitioning designs to GF 22FDX







Future Work

- System regimes matched to hardware/signal processing constrained primitives
  - Tiling, precision-constrained beamspace, RF beamforming with switched phases
  - Operation at "low enough" SNR per antenna element
  - MU-MIMO, long-range backhaul, joint communication and sensing
- Tapeout and fabrication of RF beamformers (in 22FDX) with switched phase control
  - New approaches to packaging bottleneck
  - Hardware/signal processing co-design: calibration, tiled processing architectures

Award # 2148303

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Objective

- Hardware/signal processing co-design for radical scaling beyond 100 GHz
  - Scale array size via tiling
  - Scale bandwidth by reducing dynamic range

Challenges

- Hardware is hard beyond the fundamental design challenges at mmWave
  - Availability/support of RF CMOS processes can be uncertain
  - Packaging outcomes can be uncertain, depending on vendor

Key Accomplishments

- Fundamental limits due to reduced dynamic range
  - Constraints on system operating regime
- Power-efficient RF beamforming architectures
  - Switched phase control, novel packaging approach

Future Work

- System design matched to hardware/signal processing constraints
  - Tiling, dynamic range constraints
- Power-efficient RF beamformer hardware
  - Switched phase control + dielectric lenses