X- and K-band Tunable Phase Generation Circuits for Monolithic mm-Wave Phased Arrays

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Abstract—This paper presents design and characterization of two polyphase generation circuits, operating at X and K bands. These are crucial building blocks of an intended mixed-signal scalable architecture, suitable for integration of large beamformers on silicon technologies, operating at mm-wave frequencies. Circuits are designed with a mixed-signal approach: signals and topologies are digital, but performance and accuracy are achieved with analog-IC techniques. The novel topology proposed for the phase generator bases its operation on the time delay of matched ECL inverters loaded with quasi-matched varactors. One core phase shifter generates the phase gradient step, and it is reused several times to generate eight output differential signals of different phases. Without using any inductive component, the two phase generators provide 4 bit phase resolution in the 5-17 GHz and 11-26 GHz bands requiring 534 mW and 615 mW respectively, and are excellent candidates for the silicon integration of high-density beamformers.

I. INTRODUCTION

The large bandwidth available for mm-wave radio communications and the need of directivity for extending the usable link range motivate research interest in the integration of large phased array systems. Medium- to small-size phased arrays offer beam steering capabilities, but large-size arrays are necessary to enable WAN distances: e.g., radiating 15 dBm of signal power at 44 GHz, a pair or 10×10 arrays can transmit 1 Gbit/s over a 500 m link. While most of electronics complexity and cost of such systems is in the beamforming circuitry, modern and non-expensive silicon technologies offer performances sufficient for the 30-100 GHz range and are, thus, suitable for cost reduction by means of monolithic integration of mm-wave beamformers. This is, however, very difficult with present beamsteering IC architectures [1], [2], mostly because of their intrinsic unidimensional nature. The problem can be approached efficiently with a bi-dimensional row-column architecture [3], as its complexity and size grow with \sqrt{N} for N-element arrays. The integration of very large monolithic beamformers can also benefit from the use of mixed-signal and digital blocks, instead of reactively-tuned ones: small die-area per pixel requires inductor-free designs; given the large number of array elements, the number of cascaded analog-RF stages must be minimized, as the gain variation accumulates and is very expensive to be controlled at high frequency. Larger array sizes are possible distributing LO signals as digital signals on long lines, and keeping the operation frequency of long signal/analog lines (IF) as low as possible, since attenuation is smaller and precise gain control



Fig. 1. The proposed architecture for large monolithic phased arrays. Phase generation blocks are shown in the bottom-left corner and drive the LO distribution buses on the bottom and left-hand edges.

is of simpler implementation.

The beamformer system architecture shown in Fig. 1 and described in detail in [3] bases its operation on steering the beam in altitude and azimuth by separately imposing vertical and horizontal phase gradients. This simple assumption enables a neat separation of IF and LO distribution lines, and allows improvements in both array size and maximal operation frequency by means of two techniques: shifting most of wiring complexity to the edges of the system; distributing fast LO signals on digital buses and low-frequency IF signals on analog buses. This mixed-signal technique enables RF output frequencies higher than those possible on analog transmission lines of given length and technology [3].

Making use of two LO signals and distributed doubleupconversion double-quadrature transmitters, the input I-Q IF signals are first multiplied by a vertical phase gradient, then an independent horizontal gradient is applied and summed by means of the second upconversion mixing. At each row and column front-end, the best LO phase is selected from an *n*-phase LO signal, distributed on digital LO buses on the south and west edges of the array.

The limit to scalability is set by the maximal length of analog and digital buses, and depends on the system frequency plan and available technology. However, other fundamental system limits are related to the performance of the crucial blocks generating, distributing and selecting the multiphase LO signals: this paper describes in detail design and characterization of circuits suitable for polyphase LO-signal generation, which are crucial for the integration of large beamformers based on the intended architecture and requiring LOs in X and K bands.

II. CIRCUIT DESIGN

The phase-generator function consists in creating an *n*-phase signal from an input single-phase LO; this polyphase signal is then fed to the first LO digital buses. The generation of signals of equally spaced phases must rely on the use of a phase shifter suitable for use in a periodic structure. Many phase shifters base their operation on periodic structures, such as synthetic transmission lines using lumped elements [4] or actual transmission line sections [5], with the purpose of extending the tuning range of a core phase shift block. These topologies would be able to generate poly-phase signals, but the amplitude-loss imbalance at output ports limits their use to a small number of generated phases. Moreover, the use of inductors or transmission-line sections always increases the area required for the implementation of the phase generation blocks, specially when a large number of phases, e.g. 16, has to be available simultaneously.

For generating poly-phase LO signals, which in most cases do not carry amplitude information, digital electronics building blocks can be exploited: as shown in Fig. 2(a) for a single section, the cascade of N inverters driven by an input LO signal can provide N different phases at each interface. The input-output phase difference depends directly on the output capacitive load and can be adjusted with a small varactor or, as shown, with a pair driven by one control voltage Vctrl. A similar structure, in closed-loop configuration, is known as ring VCO and may use tuned LC loads to boost inverter performance at a certain resonance frequency [1]. In open loop configuration, an input LO signal is required, but the operation frequency depends only on the phase gradient required and on the cut-off frequency of the inverters. Load-capacitance control allows to compensate process tolerances and select the desired phase shift on a frequency range which depends on the varactor tuning ratio. At very high frequencies, this approach is severely limited by the minimum delay achievable with the available inverter: fixed the frequency, there will be a minimum phase step; for a given phase step, there will be a maximal operation frequency.

For high-frequency *and* high-resolution applications, e.g. 16 phases at 30 GHz, we propose to generate different phases exploiting the phase difference at the output of two matched inverters loaded with quasi-matched varactors. As shown in



Fig. 2. Polyphase LO signal generation realized by means of tuned inverter delays: the cascade of N inverters can provide N different phases of the same signal (a); two matched inverters loaded with quasi-matched capacitors can provide small phase differences (b); implementations presented in this paper exploit ECL-logic inverters (c).



Fig. 3. System-level schematic of a 16-phase generator. Dashed box shows the details of the differential core shift element.

Fig 2(b), it is possible to increase the phase difference of two signals by an arbitrarily-small phase delay: two signals of different phases are fed into two matched inverters, loaded with two pairs of matched varactors of slightly different value. By means of a differential pair, the time delay difference can be increased and reduced around the nominal value with one control voltage. At a given frequency of operation, the phase difference between the two signals depends on the varactor control voltages and size ratio. Exploiting this basic idea, it is possible to generate 2^n phases arranging in a binary tree several blocks, each producing a $360^{\circ}/2^n$ phase shift. Fig. 3 shows the detail of a 16-phase design, based on a 22.5° building block. The circuit bases its operation on the use of one basic phase-shift block: phase matching among different instances relies on same-die matching; phase accuracy is achieved by analog continuous adjustment of the varactor, controlled by the same voltage in each instance.

Implementing the topologies shown in Fig. 2(b) and Fig. 3, two phase generators were design and fabricated, optimized for X and K bands, in order to be capable of generating 16 phases of a differential LO signal provided externally. Digital inverters are in ECL logic (Fig. 2(c)), optimized for operating at peak f_t collector current density, except the last buffer stages, designed to feed the $\pm 300 \text{ mV}$ ECL digital signal to the output 50 Ω transmission-lines. The X-band version consists of 252 *H*BTs, 192 *r*esistors and 48 *v*aractors, while the K-band version employs 372 *H*BTs, as in each core shift block an extra inverter is used before driving the varactor: this extend the phase-shifter cutoff frequency.

III. EXPERIMENTAL RESULTS

A. Fabrication

The phase generation ICs were fabricated on a commercially-available 0.18 μ m BiCMOS technology, featuring f_t =155 GHz, f_{max} =200 GHz HBTs and high-quality passive elements.

Available die area limits the number of outputs to two differential signals; the ICs were fabricated with contact pads on two quadrature signals, for characterization ease. Phase accuracy of the remaining outputs relies on same-die process tolerances.

A photograph of the X-band version is shown in Fig. 4(a): IC measures $1.34 \text{ mm} \times 0.68 \text{ mm}$, and circuit active area occupies 0.13 mm^2 . A photograph of the the K-band phase generator is in Fig. 4(b): in the same pad-limited IC area, the K-band version active area is 0.15 mm^2 .

B. Circuit Characterization

The two phase generation ICs were tested on wafer. The X-band and K-band versions require 181 mA and 205 mA of bias current, respectively, from -3 V. Output signals are two differential ECL waveforms, whose phase difference depends on a control voltage provided externally. The two output signals were observed by means of a two-channel 50 GHz sampling scope and phase differences derived as time



Fig. 4. IC photographs: phase generation ICs operating at X-band (a) and Kband (b). Die area shown measures $1.34 \text{ mm} \times 0.68 \text{ mm}$ in both cases, while active are used is 0.13 mm^2 for the X-band version and 0.15 mm^2 for the K-band version. At the highest frequency of operation, the core phase shifter needs one extra inverter to restore digital levels between stages.



Fig. 5. Unit phase shift as function of control voltage for the X-band version of the phase generator. Frequencies shown are spaced by 2 GHz.

delay measurements or Fourier analysis; the two approaches returned phase measurements consistent within $\pm 1^{\circ}$ in the band of operation, as higher order harmonics are filtered by the inverter frequency response. Results presented in this paragraph are elaboration of time delay measurements.

Fig. 5 shows the phase shift of the core shift element reused hierarchically in the X-band phase generator. The measured phase shift as function of control voltage is shown for a set of frequencies spaced by 2 GHz. In the usable band, the planned 1.1 V control range results in a 20-25° tuning range, centered around the 22.5° target. Maximal operation frequency for this circuit is 17 GHz: since the additional capacitive load of the varactors reduces inverter cutoff frequency, at frequencies higher than 17 GHz digital voltage



Fig. 6. Measured phase difference produced by the core phase shifter of the K-band phase generator. The target phase of 22.5° is selectable from 5 GHz to 17 GHz.



Fig. 7. Unit phase shift as function of control voltage for the K-band version of the phase generator. Frequencies are spaced by about 2 GHz.

levels are not reached at the output for any value of the control voltage; at the highest useable frequencies, the tuning range is progressively reduced, because of the same effect. Fig. 5 shows the frequency behavior of maximal and minimal selectable phases, together with the control voltage required for the target phase of 22.5°. The phase generator is capable of providing the required phase gradient in the 5-17 GHz band.

Fig. 7 shows measured phase shifts for the K-band version. A tuning range similar to that of the X-band version is available at an higher frequency: maximal frequency of operation for this circuit is 27 GHz. Fig. 8 shows the measured phase difference produced in the K-band IC by the core phase shifter as function of frequency; for each frequency, minimal and maximal phase shift correspond to the ends of the range achievable by tuning the varactor. The K-band phase-shift block can be set to the required 22.5° in the 11-26 GHz band.

IV. CONCLUSION

The proposed system architecture for a row/column beamformer IC bases its operation on the availability of on-chip



Fig. 8. Measured phase difference for the core phase shifter of the X-band phase generator. Useable band is 11 GHz to 26 GHz.

generated polyphase LO signals. The design and implementation of building blocks providing the phase generation function has been presented. As the row/column architecture exploits analog and digital design techniques in order to extend its scalability and operation frequency limits, the design of the phase generation components similarly benefits of both approaches. Polyphase LO signals are generated combining digital ECL inverters, but phase accuracy and control is achieved by means of on-chip device matching and continuous capacitive load tuning, i.e. analog techniques. This innovative design approach results in satisfactory performance at X and K band: without employing any inductive component, presented phase generation circuits are excellent candidates for the integration of very large mixed-signal phased arrays operating in the 30-40 GHz bands.

ACKNOWLEDGEMENT

This work was funded by the DARPA SMART program and National Science Foundation, under grants *ECS-0636621* and *CNS-0520335*. The authors wish to thank N. Desai and A. Ballinger for their assistance in characterizing the circuits.

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