On the theory of multiGigabit transceiver implementations

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***Abstract*—The analog-to-digital converter (ADC) is the fundamental bottleneck to scaling mostly digital communication transceiver architectures to multiGigabit speeds: high-precision, high-speed ADCs are too costly, too power-hungry, or simply not available. One possible approach to this problem is to use drastically lower ADC precision in the receiver. However, the insertion of a severe nonlinearity in the transceiver chain implies that we must comprehensively rethink signal processing for communication, which is largely based on linear models. After reviewing what Shannon theory tells us, we discuss recent results on demodulation, automatic gain control, and transmit precoding.**

I. Introduction

The revolution in cellular and wireless local area network (WLAN) technology over the past two decades has been driven by the migration to "mostly digital" architectures for communication transceivers. Such architectures, which are predicated on the availability of accurate analog-to-digital conversion, allow us to leverage Moore's law to achieve sophisticated signal processing functionalities in the digital domain. In this paper, we report on a body of work resulting from the following question: can we still enjoy the benefits of the economies of scale provided by mostly digital architectures as communication bandwidths of a Gigahertz or more? Potential applications include multiGigabit wireless communication using the unlicensed 60 GHz band, and upgrades of optical communication technology to larger constellations. Moore's law is still working in our favor in such settings: more and more transistors that are faster and faster can be packed into an integrated circuit, and can be used to perform digital signal processing at multiGigabit speeds. The bottleneck now becomes the ADC: high-precision, high-speed ADCs are too costly and too power-hungry, or simply not available [1].

The short-term approach to the ADC bottleneck is to go back to employing analog processing; for example, instead of quantizing after the sampler, we would work directly with continuous-valued samples. However, this calls for hand-crafted mixed signal designs which do not take advantage of Moore's law. A longer term solution is to modify communication transceiver design to accommodate constraints on ADC capability. In particular, one possibility is to employ ADCs with precision of 1-4 bits, rather than the 8-12 bits of precision used in typical implementations today. Such a drastic reduction in precision means that we are introducing a severe nonlinearity prior to digital signal processing (DSP) at the receiver. This requires a comprehensive rethinking of communication transceiver design, since the state of the art is based largely on linear models. In this paper, we summarize recent results on communication transceiver design with low-precision ADC, and comment on possible directions for future research. We begin by noting that Shannon theory tells us that, for an idealized channel model, the loss due to low ADC precision is moderate. This motivates research into the design of signaling schemes and receiver processing algorithms. Our preliminary results on the latter show that dithering and feedback play a critical role.

II. Shannon-Theoretic Limits

We began by looking at what happens when we quantize the output of a real-valued, discrete-time AWGN channel, which might arise, for example, from Nyquist rate sampling of a system with no intersymbol interference (ISI), ideal timing synchronization and ideal carrier synchronization, in which case the in-phase (I) and quadrature (Q) components can be processed separately. Thus, if we send a stream of symbols $\{X[k]\}$, we receive

$$Y[k] = \mathcal{Q}(X[k] + N[k])$$

where $\mathcal{Q}(\cdot)$ is the quantizer and $\{N[k]\}$ are i.i.d. zero mean Gaussian noise samples. Our main results [2], [3] are as follows:

(a) If the quantizer has K bins, then the optimal input distribution need not have any more than $K+1$ points (in our numerical optimization of input distribution, we find that K points suffice).

(b) Uniform Pulse Amplitude Modulation (PAM) with quantizer boundaries chosen to coincide with maximum likelihood (ML) decision boundaries is near-optimal.

(c) Even for moderately high signal-to-noise ratio (SNR) of up to 20 dB, 2-3 bit quantization results in only 10-20% reduction of spectral efficiency compared to unquantized observations.

Our next step was to investigate the effect of carrier synchronization, assuming that everything else is ideal. Standard techniques for estimating and compensating for carrier frequency offset in DSP are no longer applicable when the receiver ADC precision is constrained. However, for typical carrier frequency offsets, the carrier phase can be modeled as constant (but unknown) over several symbols. We have used

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the resulting *quantized* block noncoherent channel model to derive Shannon-theoretic insights that say that carrier synchronization is not a fundamental bottleneck [4], and to show that dithering at the transmitter can be used to break unwanted symmetries.

III. Signal Processing Architectures

The Shannon theory results of the previous section pertain to a non-dispersive channel. For even moderately dispersive channels, it is intuitively clear that we would require ADCs with larger dynamic range in order to obtain enough information to undo the effects of ISI. However, it may be possible to sidestep this problem by moving ISI compensation to the transmitter: in general, high-speed digital-to-analog converters (DACs) are easier to realize than high-speed ADCs. Figure 1 shows the architecture that we envision. The receiver must perform its usual functions of carrier synchronization (implicit or explicit), timing synchronization and AGC. Furthermore, it estimates the channel and feeds back its estimates to the transmitter, which performs precoding to alleviate ISI and to reduce the dynamic range requirements at the receiver. Such an architecture is particularly well matched to scenarios where the transmitter is more capable than the receiver; for example, a laptop transmitting to a handheld over a short-range 60 GHz link. However, how does the receiver perform functions such as channel estimation and AGC when it only has a few bits of precision? The answer is to dither the input to the ADC.

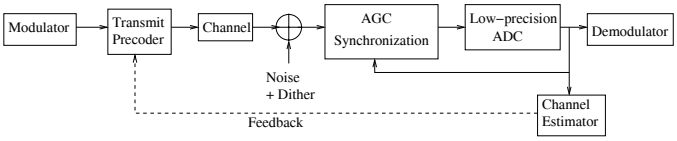

Fig. 1. Possible transceiver architecture for communication over a dispersive channel when the receiver employs low-precision ADC.

For channel estimation [5], consider multiple noisy observations of a single coefficient h. (See [5] for an explanation of how we can focus on one coefficient at a time, without loss of generality.) We assume that we can scale and dither the input to the ADC to get the following sequence of observations:

$$Y_k = \mathcal{Q}\left(G_k(h + N_k + D_k)\right) \quad , \quad k = 1, 2, ...$$

where $\{N_k\}$ is the i.i.d. zero mean Gaussian noise sequence, and $\{G_k\}$ and $\{D_k\}$ are gain and dither sequences under our control. We have shown in [5] that the following design works: choose the dither D_k to be negative of the linear minimum mean squared error (LMMSE) estimate of h based on the observations $Y_1, ..., Y_{k-1}$, so that we are quantizing the *error* in the LMMSE estimate, and choose the gain G_k so as to scale the error in order that the dynamic range of the quantizer is fully utilized. This is reminiscent of sigma-delta quantization, and is an example of choosing dither sequences as a function of the received signal.

As an example of a different kind of dithering, consider the problem of automatic gain control in the following simple setting: 4-ary pulse amplitude modulation (4PAM) signaling in WGN, with decisions to be made after a 2-bit ADC. We know from [3] that, if the quantizer thresholds coincide with the ML decision boundaries, then the system is near-optimal. The job of AGC, therefore, is to scale the input to the ADC to achieve this. To do this, we must estimate the unknown signal amplitude. We have shown that amplitude estimation based on the ADC input performs poorly at high SNR, but that adding a white noise dither (independent of the received signal) to the input of the ADC resolves the problem. Details of this work will be presented at the conference, and will be reported in a separate publication.

Finally, in recent work, we have shown that transmit precoding is indeed effective in combating ISI when the receiver employs low-precision ADC. Results from this preliminary work will also be presented at the conference.

IV. Conclusions

The ADC bottleneck implies that we must rethink all aspects of transceiver design for multiGigabit communication. Our preliminary results attack pieces of this problem, such as channel estimation, AGC, and carrier synchronization. Dithering emerges as a recurring theme, providing a mechanism for extracting more information out of a limited number of quantization bins. The challenge now is to integrate these ideas into complete link designs. One interesting test case is the design of line-of-sight 60 GHz links with directional transmission and reception, where there is a limited amount of channel dispersion that we need to handle.

While we focus on low-precision ADC here, it is worth noting that it may be possible to increase dynamic range using time-interleaved ADC architectures employing a number of low-speed, high-precision ADCs. The problem now is to eliminate the performance degradation due to the mismatch between the parallel ADCs [6].

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