# An 18-dBm, 57 to 85-GHz, 4-stack FET Power Amplifier in 45-nm SOI CMOS

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***Abstract*—A single stage, 4-stack FET SOI CMOS power amplifier (PA) demonstrates to the author's knowledge the widest bandwidth covering 57 through 85 GHz for a CMOS PA while delivering a peak 18 dBm of output power. The 4-stack topology is also demonstrated for the first time in W-band to provide high output voltage swing while avoiding premature device aging and breakdown. The wideband performance results from a proposed series-shunt interstage matching network between the stacked FETs. The PA achieves a peak PAE of 20% and 12-dB gain with a 4.8-V power supply. The millimeter-wave PA is implemented in GlobalFoundries 45-nm SOI CMOS technology using a trap-rich substrate. A compact chip area of 525 $\mu$m $\times$ 300 $\mu$m is shown excluding pads.**

***Index Terms*—wideband, fractional bandwidth, stacked FET, mm-wave PA, CMOS, CMOS SOI.**

## I. Introduction

SOI CMOS has attracted attention for millimeter-wave power amplifiers due to the ability to series power combine through floating body transistor stacking while also allowing wideband matching [1], [2] and high voltage swing [3]. In [2], a formula for designing high efficiency stacked-FET PA with interstage matching was derived and a PA with19-dBm $P_{sat}$ and peak PAE of 14% was been demonstrated at 91 GHz. Recently, a 3-stacked PMOS PA was demonstrated at E-band that offered excellent output power and PAE with the improved reliability from PMOS devices in 32-nm SOI CMOS technology [4]. Here, we demonstrate an extremely wideband (40% fractional bandwidth) PA in 45-nm SOI CMOS with the capability of covering WiGiG (57-64 GHz), the recently allocated unlicensed band between 64-71 GHz, and existing E-band allocations (71-76 GHz and 81-86 GHz). To the best of our knowledge, this is the highest FBW CMOS millimeter-wave PA and the first to demonstrate the capability to cover all of these bands.

This work proposes a new shunt-series interstage matching network for stacked FET PAs. At high frequency, loss from passive components significantly reduces PA efficiency. Therefore, the proposed wideband interstage matching networks avoids excessive loss associated with large numbers of passive elements in the matching network. Additionally, we demonstrate the effectiveness of this wideband matching network by demonstrating a 4-stack FET PA. To our knowledge, no prior work has demonstrated 4 stacks above 60 GHz. Stacking more transistors has the benefit of reducing the voltage swing on individual devices while delivering a given output power for better reliability and aging.

Section II describes the proposed PA and the interstage matching network based on an analysis of the impedance variation across frequency seen between series combined transistors. In Section III, a 4-stacked FET PA is presented for operation from 57 GHz to 86 GHz. Section IV presents the measurement results and illustrates excellent agreement compared to simulations with a bandwidth of 58 GHz to 85 GHz. Additionally, we present a table of comparison to illustrate the performance relative to other CMOS technologies.

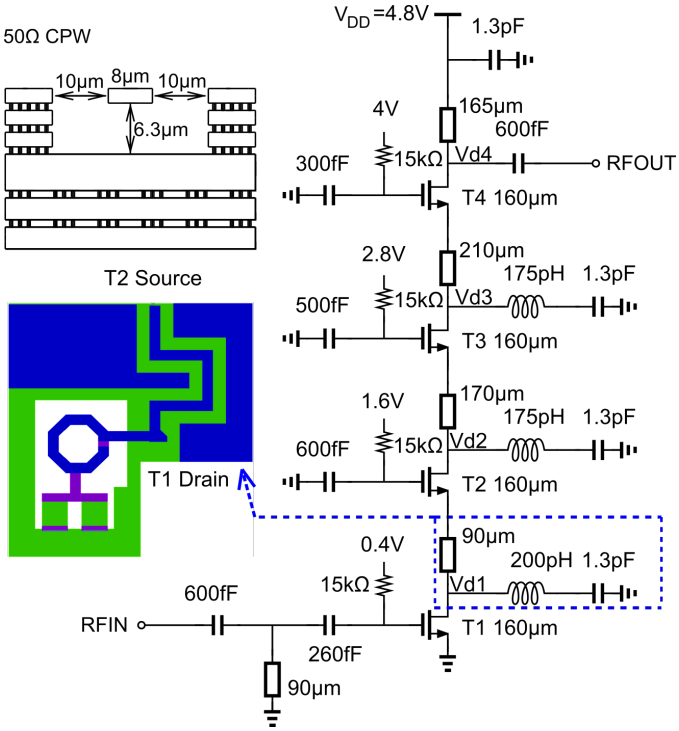


Fig. 1. Schematic of the 57-85 GHz 4-stacked FET power amplifier

## II. Wideband Impedance Matching

Fig. 1 shows the 4-stacked FET PA. The input is a common-source FET and three additional stacked FETs are used to increase the voltage handling of the PA. To avoid breakdown, the rms $V_{ds}$ swing and $V_{gd}$ swing should be constrained below 2.5V and DC voltage supply for a single FET should not exceed 1.4V for the 45-nm CMOS SOI process [2], [3]. However, these high DC supply voltages could induce hot carrier injection which prematurely ages the device and lower supplies are preferred suggesting stacking more transistors for a given supply. The gate capacitor and $C_{gs}$ form a capacitive voltage divider that allows an AC swing on the gate in phase with the source and drain signal swings. The

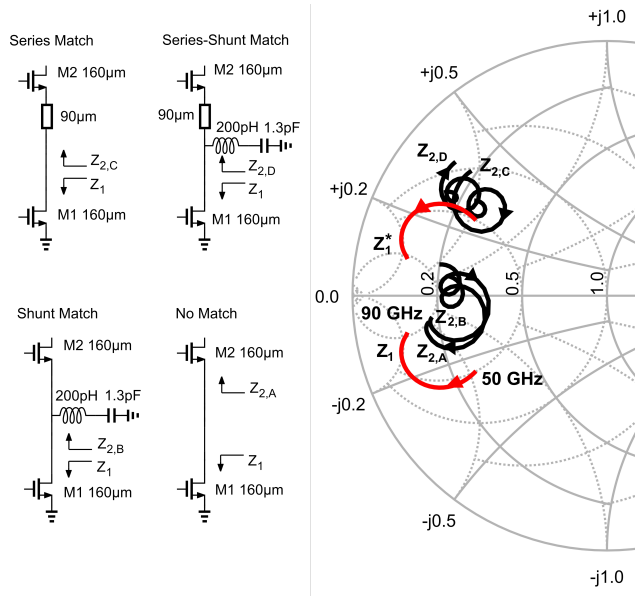


Fig. 2. Interstage impedance matching using a combination of series and shunt components

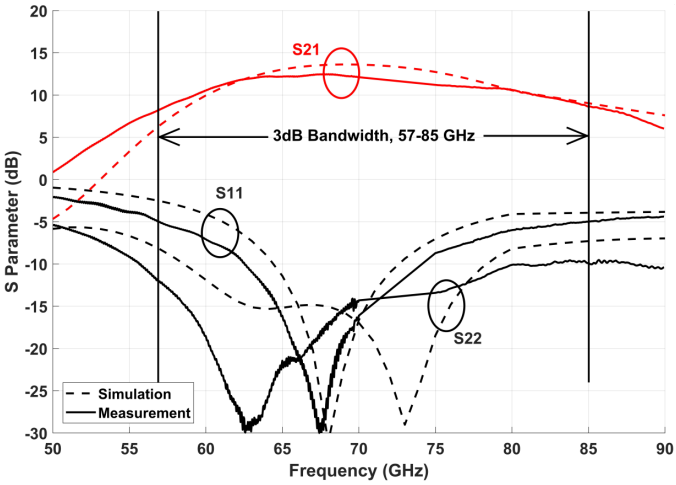


Fig. 3. Simulated and measured S-parameters, Psat and PAE

instantaneous gate-drain voltage as well as the drain-source voltage are reduced by keeping all voltages in-phase. Smaller gate capacitance becomes necessary as the gate voltage swing requirement increases for the top-most FETs in the stack.

Fig. 2 no matching plots the drain terminal impedance looking into the common source FET transistor ($Z1$) and the source terminal impedance looking into the common gate FET transistor ($Z2$) from 50 GHz to 90 GHz. For ideal power matching, these impedance should be complex conjugates of one another. However, at high frequency, the drain and source impedance become increasingly capacitive and, consequently, the drain and source terminal do not exhibit power matching.

Comparing the $Z1$ and $Z2$ impedance curves on the Smith chart, the real part of the impedance remains similar at both terminals across a relatively wide frequency range. This suggests that only reactive matching is required for wideband operation. In prior work, either a shunt or series interstage matching network was used to implement the PA. If only a shunt inductor is used for matching, the imaginary part of the impedance can be cancelled only valid over a relatively narrow bandwidth. In Fig. 2 shunt matching, a shunt 50 pH inductor is added in the interstage matching network resulting in a network that does not produce wideband interstage matching.

If a series inductor is used for interstage matching, as shown in Fig. 2 series matching, it introduces a significant increase in the impedance at higher frequencies and the high frequency region is more inductive than required for matching to the source impedance.

The proposed approach combines these two techniques to use a shunt inductor and series transmission line as shown in Fig. 2 series-shunt matching. This combination offers optimal power matching over a wider frequency range as exhibited by the conjugate power matching of $Z1$ with respect to $Z2$ on the Smith chart. The matching elements in this simulation include a 200 pH inductor and 90um series transmission line. While the figure illustrates the interstage matching between the common source and common gate transistors, similar interstage matching behavior is exhibited between the stacked FETs, demanding a similar interstage matching network.

## III. Circuit Implementation

The power amplifier was designed with using Global Foundries 45nm SOI CMOS process with 11 metal layer option and a trap-rich substrate. The top metal layer is 2.2um thick and is used for the signal line ground CPW transmission lines as well as inductors. EM simulations indicate the inductor Q with the trap-rich substrate is as high as 20.

In the 4-stacked FET PA, each FET is 160$\mu$m wide with a 40nm gate length. For the highest gain, the transistor is biased in class AB region where the load line of a 40$\mu$m wide transistor is close to 50 Ohms. Consequently, choosing 160$\mu$m exhibits a load line for the composite 4-stack device that is also approximately 50 Ohms while allowing increasing the output power by 12 dB. Each NFET in the stack is modeled by PEX to include the poly to active region parasitic capacitance and bottom routing parasitics up to M2 while the passive interconnections above M2 were modeled using EMX.

With proper FET sizing, gate capacitors are chosen to ensure each drain to gate voltage swing does not exceed 2.5V and NFETs experience similar drain-to-source voltage swings. The shunt inductance was implemented as a single-turn inductor to reduce the chip area. However, the series inductance was implemented as a transmission line to distribute the heat generated from each of the transistors.

## IV. Measurement Results

The chip micrograph is shown in Fig. 8. The PA area is 525 $\mu$m $\times$ 300 $\mu$m excluding pads. The PA has been measured using a Keysight 5247 network analyzer to 67 GHz and from 75 GHz to 110 GHz with frequency extenders. The simulated and measured $\boldsymbol{S}$-parameters of the PA with a

TABLE 1

| Param.\Ref. | [4] | [5] | [6] | [7] | [8] | **This work** |
|---|---|---|---|---|---|---|
| Tech CMOS | 32nm SOI | 14nm FinFET | 40nm | 65nm | 28nm SOI | **45nm SOI** |
| Supply (V) | -3.6 | 1 | 0.9 | 1.3 | 1 | **4.8** |
| Frequency (GHz) | 65-92 | 67-75.5 | 59-67 | 68-78 | 55-65 | **57-85** |
| FBW (%) | 34 | 12 | 12.7 | 13.7 | 16.7 | **39.4** |
| $P_{sat}$ (dBm) | 19.6 | 7.4 | 16.4 | 17.3 | 18.8 | **18** |
| $P_{1dB}$ (dBm) | - | 2 | 13.9 | 14.6 | 18.2 | **15** |
| Peak PAE (%) | 18 | 8.9 | 23 | 18.9 | 21 | **20** |
| Chip Size ($mm^2$) | 0.12 | 0.1 | 0.09 | 0.09 | 0.162 | **0.15** |
| FOM**1** | 261 | 250 | 268 | 268 | 263 | **260** |
| FOM**2** | 73.8 | 55 | 74.3 | 74.2 | 71.8 | **74.9** |

$$FOM1(ITRS) = P_{sat} + Gain + 10log(PAE_{peak}) + 20log(Freq)$$
$$FOM2 = P_{sat} + Gain + 10log(PAE_{peak}) + 20log(FBW)$$

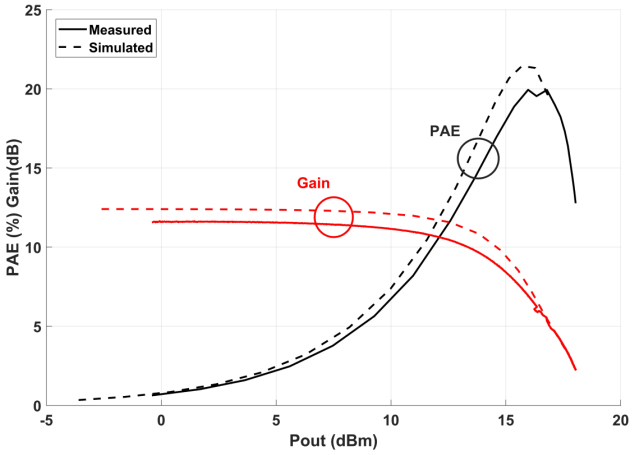


Fig. 4. Measured large signal performance of proposed PA at 64 GHz

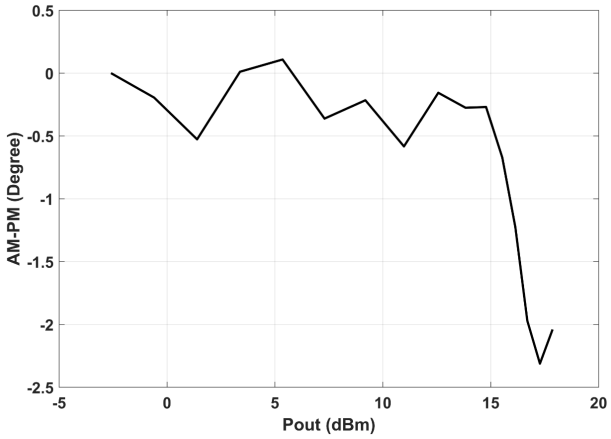


Fig. 6. Measured large signal performance of proposed PA at 64 GHz

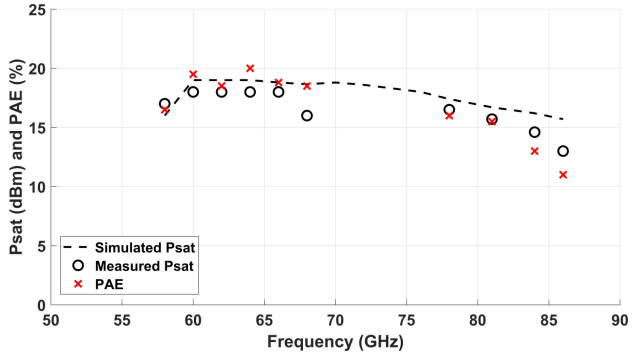


Fig. 5. Simulated and measured Psat and PAE

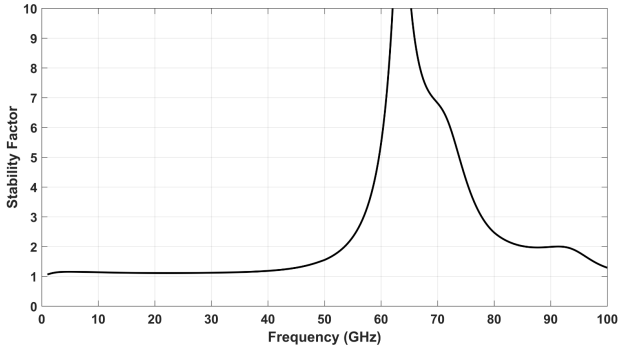


Fig. 7. Stability $\mu$ factor

4.8V supply are shown in Fig. 3 and compared against circuit simulations. Notably, the PA exhibits excellent agreement of the gain and input and output return loss across 50-90 GHz. At 70 GHz, the measurements indicate a 1-dB gain reduction compared to simulation which results from under-estimated loss in the passive device modeling due to the trap-rich substrate modeling. Additionally, the $S22$ shifts to a lower frequency range due to the output bypass capacitance. The peak measured small signal gain is 12 dB and the 3-dB small signal bandwidth extends from 57 to 85 GHz.

The PA achieves a peak saturated output power ($P_{sat}$) of 18 dBm and a peak PAE of 20% at 64GHz. Fig. 4 shows saturated output power ($P_{sat}$) change with frequency. Fig. 5 shows the efficiency and gain compression as a function of the output power ($P_{out}$).Fig. 6 shows AM-PM characteristic and indicates the soft compression of the PA phase change of 3 degree. Fig. 7 shows the stability $\mu$ factor from DC to 100 GHz. The circuit is unconditional stable. Table I shows a performance comparison with recently published results based on CMOS process technologies. To the best of our knowledge, this PA presents reasonable output power and efficiency with a record fractional bandwidth of 40% from 55-85 GHz.

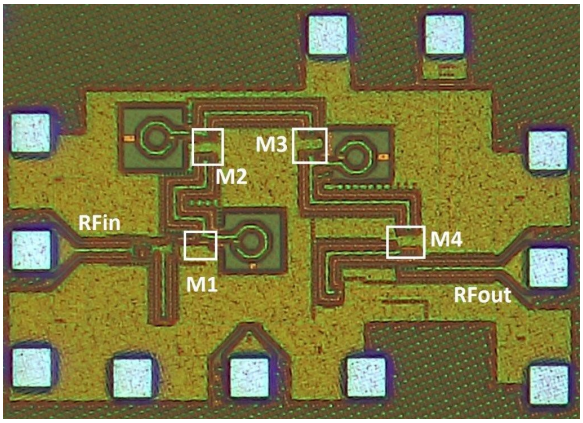


Fig. 8. Microphotograph of the 4-stack FET PA

## V. Conclusion

A single-stage 4-stacked FET 45-nm SOI CMOS power amplifier is presented. Based on power matching of the interstage FET network at millimeter-wave bands, we propose a new interstage matching network based on a combination of series and shunt components that achieves a high fractional bandwidth. The measurement results verify the wideband operation and demonstrate performance that covers existing 57-64 GHz, 64-71GHz, and 71-86 GHz bands while maintaining high power of 18 dBm and efficiency of 20% at 64 GHz.

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